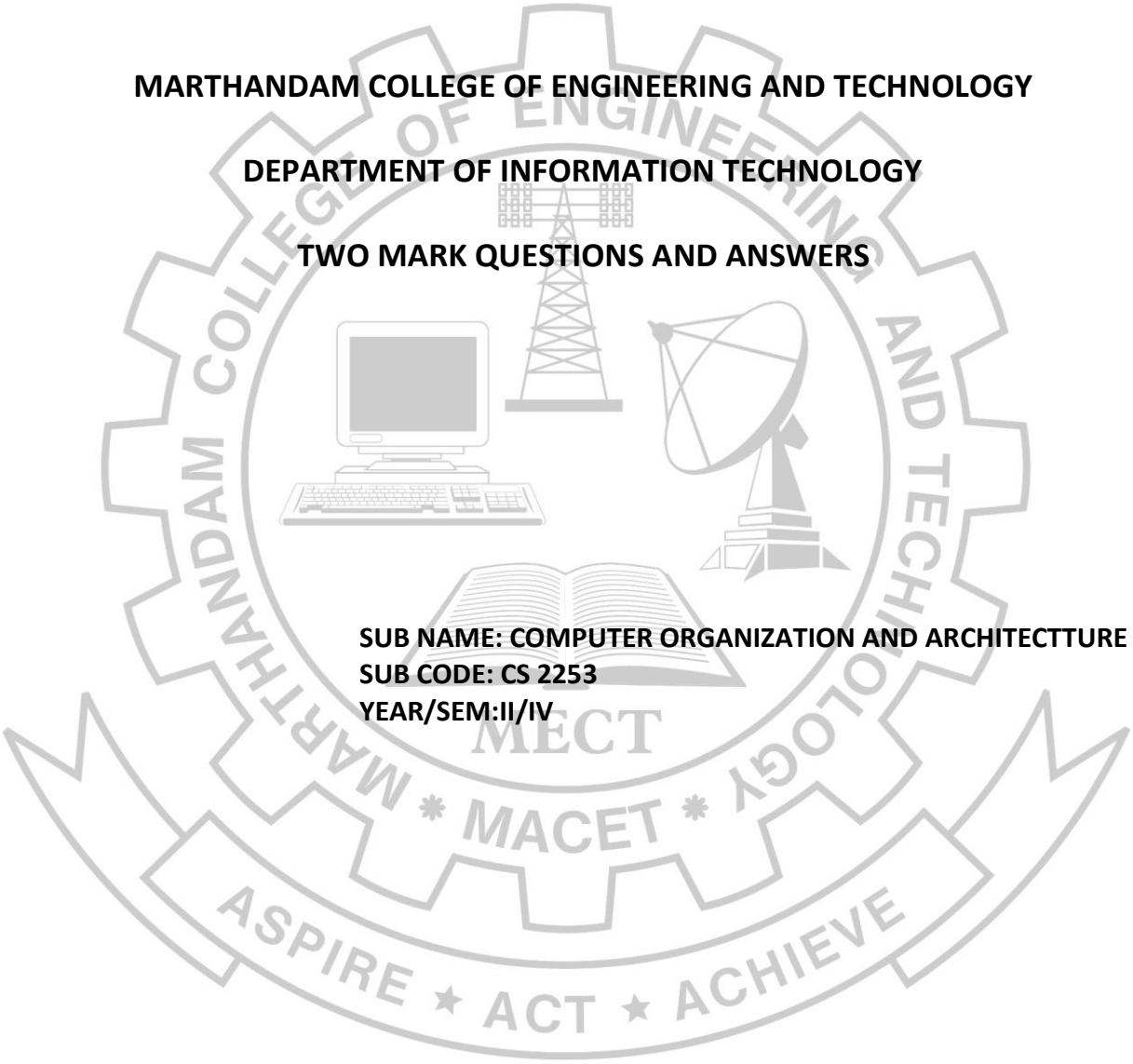
MARTHANDAM COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF INFORMATION TECHNOLOGY

TWO MARK QUESTIONS AND ANSWERS



SUB NAME: COMPUTER ORGANIZATION AND ARCHITECTTURE
SUB CODE: CS 2253
YEAR/SEM:II/IV

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CS 2253 – Computer Organization and Architecture

UNIT-I

1. What is application software? Give example.

Application programs are usually written in a high level programming language, in which the programmer specifies mathematical or text processing operations. These operations are described in a format that is independent of the particular computer used to execute the program.

Ex: C,C++,JAVA

2. What is compiler?

A system software program called a compiler translates the high-level language program into a suitable machine language program containing instruction such as the Add and
Load instructions.

3. Discuss about OS as system software?

OS is a large program or actually a collection of routines, that is used to control the sharing of and interaction among various computer units as they execute application programs. The OS routines perform the tasks required to assign computer resources to individual application programs.

4. What is text editor?

It is used for entering and editing application programs. The user of this program interactively executes command that allow statements of a source program entered at a keyboard to be accumulated in a file.

5. What are the registers generally contained in the processor?

MAR-memory address
register MDR-memory data
register IR-Instruction
Register RO-Rn-General
purpose register PC-Program
counter

6. What are the steps in executing the program?

1.fetch
2.deco
de
3.exec
ute
4.store

7. Define interrupt and ISR?

An interrupt is a request from an I/O device for service by the processor. The processor provides the requested service by executing the interrupt service routine.

8. What are condition code flags?

The processor keeps track of information about the results of various operations for use by subsequent conditional branch instructions. This is accomplished by recording the required information in individual bits, often called condition code flags.

9. What is the use of buffer register?

The buffer register is used to avoid speed mismatch between the I/O device and the processor.

10. Compare single bus structure and multiple bus structure?

A system that contains only one bus(i.e only one transfer at a time) is called as a single bus structure. A system is called as multiple bus structure if it contains multiple buses.

11. What is multiprogramming or multitasking?

The operating system manages the concurrent execution of several application programs to make the best possible uses of computer resources. This pattern of concurrent execution is called multiprogramming or multitasking.

12. What is elapsed time of computer system?

The total time to execute the total program is called elapsed time. it is affected by the speed of the processor, the disk and the printer.

13. What is processor time of a program?

The periods during which the processor is active is called processor time of a program it depends on the hardware involved in the execution of individual machine instructions.

14. Define clock rate?

The clock rate is given by, R=1/P, where P is the length of one clock cycle.

15. Write down the basic performance equation?

T=N*S/R
T=processor time
N=no.of
instructions S=no
of steps R=clock
rate

16. What is branch target?

As a result of branch instruction, the processor fetches and executes the instruction at a new address called branch target, instead of the instruction at the location that follows the branch instruction in sequential address order.

17. Define addressing modes.

The different ways in which the location of an operand is specified in an instruction are referred to as addressing modes.

18. What is index register?

In index mode the effective address of the operand is generated by adding a constant value to the contents of a register. The register used may be either a special register or

may be any one of a set of general purpose register in the processor. This register is referred to as an index register.

19. What is assembly language?

A complete set of symbolic names and rules for the use of machines constitute a programming language, generally referred to as an assembly language.

20. What is loader?

Loader is a system software which contains a set of utility programs. It will load the object program to the memory.

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UNIT II

1. Define data path.

The registers, the ALU, and the interconnecting bus are collectively referred to as the data path.

2. Explain MDR and MAR.

The data and address lines of the external memory bus connected to the internal processor bus via the memory data register, MDR,and the memory address register , MAR,respectively. Register MDR has two inpits and two outputs.

Data may be loaded into MDR either from the memory bus or from the internal processor bus the data stored in MDR may be placed on either bus. The input of MAR is connected to the internal bus and it's output is connected to the external bus.

3. Define processor clock.

Processor clock is defined as the time periods in which all operations and data transfer with in the processor take place.

4. What is known as multiphase clocking?

When edge-triggered flip flops are not used, two or more clock signals may be needed to guarantee proper transfer of data. This is known as multiphase clocking.

5. Define MFC.

To accommodate the variability in response time, the processor waits until it receives an indication that the requested read operation has been completed. The control signal used for this purpose is known as memory-function-completed(MFC).

6. What is WMFC?

WMFC if the control signal that causes the processor's control circuitry to wait for the arrival of the MFC signal.

7.What is meant by branch instruction?

A branch instruction is an instruction which replaces the contents of the PC with the branch target address. This address is usually obtained by adding offset X, which is given in the branch instruction is called a branch delay slot.

8.What are the two approaches used for generating the control signals in proper sequence?

- Hardwired control
- Microprogrammed control

10. Explain hardwired control.

The control hardwire can be viewed as the state machine that changes from one state to another in every clock cycle, depending on the contents of the instruction register, the condition codes and the external inputs. The outputs of the state machine are the control signals.

The sequence of operations carried out by this machine is determined by the writing of the logic elements, hence the name "hardwired".

10. What are the features of the hardwired control?

A controller that uses this approach can operate at high speed. It has little flexibility and the complexity of the instruction set it can implement is limited.

11. What is micro programmed control?

Micro programmed control is a scheme in which control signals are generated by a program similar to machine language program.

12. What is control word?

A control word is a word whose individual bits represent the various control signals.

13. Define microroutine and microinstruction.

A sequence of control words corresponding to the control sequence of a machine instruction constitutes the microroutine for that instruction and the individual control words in this microroutine are referred to as microinstructions.

14. What is control store?

The microroutines for all the instructions in the instruction set of a computer are stored in a special memory called the control store.

15. What is the drawback of assigning one bit position to each control signals?

Assigning individual bits to each control signal results in long microinstructions because the number of required signals is usually large.

Moreover, only a few bits are set to "1" in any given microinstruction, which means the available bit space is poorly used.

16. Name some register output control signals.

Pc $_{out}$, MDR $_{out}$, Z $_{out}$, Offset $_{out}$, R1 $_{out}$, R2 $_{out}$, R3 $_{out}$ and TEMP $_{out}$.

17. What is vertical organization and horizontal organization?

Highly encoded schemes that use compact codes to specify only a small number of control functions in each microinstruction are referred to as vertical organization. On the other hand, the minimally encoded scheme in which many resources can be controlled with single microinstructions is called a horizontal organization.

18. Compare vertical organization and horizontal organization Vertical organization Horizontal organization

• Highly encoded schemes.

• Specify only a small number of Minimally encoded schemes. Many resources can be controlled.
control signals.

• Operating speed is high. Operating speed is low.

20. What is the draw back of micro programmed control?

It leads to a slower operating speed because of the time it takes to fetch microinstructions from the control store.

20. Define emulation.

Given a computer with a certain instruction set, it is possible to define additional machine instructions and implement them with extra micro routines. Emulation allows us to replace obsolete equipment with more up to date machines. If the replacement computer fully emulates the original one, then no software changes have to be made to run existing programs. Thus, emulation facilitates transitions to new computer systems with minimal distribution.

UNIT III

1. What is imprecise and precise exception?

Situation in which one or more of the succeeding instructions have been executed to completion is called imprecise exception. Situation in which all subsequent instructions that may have been partially executed are discarded. This is called a precise exception.

2. What are the major characteristics of a pipeline?

The major characteristics of a pipeline are:

a) Pipelining cannot be implemented on a single task, as it works by splitting multiple

tasks into a number of subtasks and operating on them simultaneously.

b) The speedup or efficiency achieved by suing a pipeline depends on the number of pipe stages and the number of available tasks that can be subdivided.

c) If the task that can be subdivided has uneven length of execution times, then the speedup of the pipeline is reduced.

d) Though the pipeline architecture does not reduce the time of execution of a single task, it reduces the overall time taken for the entire job to get completed.

3. What are the types of pipeline hazards?

The various pipeline hazards are:

1. Data hazard
2. Structural Hazard
3. Control Hazard.

4. What is a pipeline hazard?

Any condition that causes the pipeline to stall is called hazard. They are also called as stalls or bubbles.

5. Name the four steps in pipelining.

Fetch : Read the instruction from the memory.

Decode : Decode the instruction and fetch the source operand. Execute : Perform the operation specified by the instruction. Write : Store the result in the destination location.

6. What is the use of cache memory?

The use of the cache memories solves the memory access problem. In particular, when a cache is included on the same chip as the processor, access time to cache is usually the same as the tine needed to perform other basic operations inside the processor. This makes it possible to divide instruction fetching and processing into steps that are more or less equal in duration. Each of these steps is performed by a different pipeline stages, and the clock period is chosen to correspond to the longest one.

7. What is data hazard?

Any condition that causes the pipeline to stall is called a hazard. A data hazard is any condition in which either the source or destination operands of instruction are not available at the time expected in the pipeline. As a result some operation has to be delayed, and the pipeline stalls.

8. What are instruction hazards?

The pipeline may also be stalled because of a delay in the availability of an instruction. For example, this may be a result of a miss in the cache, requiring the instruction to be fetched from the main memory. Such hazards are often called control hazards or instruction hazards.

9. What are called stalls?

An alternative representation of the operation of a pipeline in the case of a cache miss gives the function performed by each pipeline stage in each clock cycle. The periods in which the decode unit, execute unit and the write unit are idle are called stalls. They are also referred to as bubbles in the pipeline.

10. What is structural hazard?

Structural hazard is the situation when two instructions require the use of a given hardware resource at the same time. The most common case in which this hazard may arise is in access to memory.

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11. What is said to be side effect?

When a location other than one explicitly named in an instruction as a destination operand is affected, the instruction is said to have a side effect.

12. What is dispatch unit?

A separate unit which we call the dispatch unit takes instructions from the front of the queue and sends them to the execution unit. The dispatch unit also performs the decoding function.

13. What is branch folding?

The instruction fetch unit has executed the branch instruction concurrently with the execution of other instructions. This technique is referred to a branch folding.

14. What are the two types of branch prediction techniques available?

Ans: The two types of branch prediction techniques are

1) Static branch prediction
2) Dynamic branch prediction

15. What is delayed branching?

A technique called delayed branching can minimize the penalty incurred as a result of conditional branch instructions. The idea is simple. The instructions in the delay slots are always fetched. Therefore, we would like to arrange for them to be fully executed whether or not the branch is taken. The objective is to be able to place useful instructions in these slots. If no useful instructions can be placed in the delay slots, these slots must be filled with NOP instructions.

16. What is called static and dynamic branch prediction?

The branch prediction decision is always the same every time a given instruction is executed. Any approach that has this characteristic is called static branch prediction. Another approach in which the prediction decision may change depending on execution history is called dynamic branch prediction.

17. What are condition codes?

In many processors, the condition code flags are stored in the processor status register. They are either set are cleared by many instructions, so that they can be tested by subsequent conditional branch instructions to change the flow of program execution.

18. What are superscalar processors?

Several instructions start execution in the same clock cycle, and the processor is said to use multiple issue. Such processors are capable of achieving an instruction execution throughput of more than one instruction per cycle. They are known as superscalar processors.

19. What is commitment unit?

When out-of-order execution is allowed, a special control unit is needed to guarantee

in-order commitment. This is called the commitment unit. It uses queue called the recorder buffer to determine which instruction should be committed next. Instructions are entered in the queue strictly in program order as they are dispatched for execution.

20. What is a deadlock?

A deadlock is a situation that can arise when two units, A and B use a shared resource. Suppose that unit B cannot complete its task until unit A completes its task. At the same time, unit B has been assigned a resource that unit A needs. If this happens, neither unit can complete its task. Unit A is waiting for the resource it needs, which is being held by unit B at the same time, unit B is waiting for unit A to finish before it can release that resource.

UNIT IV

1.Define static memories?

Memories that consists of circuits capable of retaining their state as long as power is applied is called static memories

2.What are the characteristics of semiconductor RAM memories?

- They are available in a wide range of speeds.
- Their cycle time range from 100ns to less than 10ns.
- They replaced the expensive magnetic core memories
- They are used for implementing memories.

4. Define Refresh Circuits?

It is a circuit which ensures that the contents of a DRAM are maintained when each row of cells are accessed periodically.

4. Define Memory Latency?

It is used to refer to the amount of tile it takes to transfer a word of data to or from the memory.

5. What is asynchronous DRAM?

In asynchronous DRAM, the timing of the memory device is controlled asynchronously. A specialized memory controller circuit provides the necessary control signals RAS and CAS that govern the timing. The processor must take into account the delay in the response of the memory such memories are asynchronous DRAM.

6. Define Bandwidth?

When transferring blocks of data, it is of interest to know how much time is needed to transfer an entire block, since blocks can be variable in size it is useful to define performance measure in terms of number of bits or bytes that can be transferred in one second. This measure is often referred to as the memory bandwidth.

7. What is double data rate SDRAM?

Double data rates SDRAM are those which can transfer data on both edges of the clock and their bandwidth is essentially doubled for long burst transfers.

8. Want is mother board?

Mother Board is a main system printed circuit board which contains the processor. It will occupy an unacceptably large amount of space on the board.

9. What are SIMM and DIMM?

SIMM are Single In-Line Memory Module.DIMM is Dual In-Line Memory Modules. Such modules are an assembly of several memory chips on a separate small board that plugs vertically into a single socket on the motherboard.

10. Differentiate static RAM and dynamic RAM?

S.NO	STATIC RAM	DYNAMIC RAM

1	They are fast	They are slow
2	They are very expensive	They are less expensive
3	They retain their state indefinitely	They do not retain their state indefinitely
4	They require several transistors	They require less no transistors
5	Low density	High density

11. Define ROM?

It is a non-volatile memory. It involves only reading of stored data.

12. What are the features of PROM?

- They are programmed directly by the user.
- Faster
- Less expensive
- More Flexible

13. Why EPROM chips are mounted in packages that have transparent window?

Since the erasure requires dissipating the charges trapped in the transistors of memory cells. This can be done by exposing the chip to UV light.

14. What are disadvantages of EPROM?

The chip must be physically removed from the circuit for reprogramming and its entire contents are erased by the UV light.

15. What are advantages and disadvantages of using EEPROM?

The Advantages are that EEPROM do not have to be removed for erasure. Also it is possible to erase the cell contents selectively. The only disadvantage is that different voltages are needed for erasing, writing and reading the stored data.

16. What is cache memory?

It is a small, fast memory that is inserted between large, slower main memory and the processor. It reduces the memory access time

17. Define Flash Memory.

It is an approach similar to EEPROM technology. A flash cell is based on a single transistor controlled by trapped charge just like an EEPROM cell.

18. What is locality of reference?

Analysis of program shows that many instructions ion localized areas of the program are executed repeatedly during some time period, and the remainder of the program, accessed relatively infrequently. This is referred to as locality of reference. This property leads to the effectiveness of cache mechanism.

19. What are the two aspects of locality of reference? Define them.

Two aspects of locality of reference are temporal aspects and spatial aspect.

- Temporal aspect is that a recently executed instruction is likely to be executed again very soon.
- The spatial aspect is that instructions in close proximity to recently executed instructions are also to be executed soon

20. What is write-through protocol?

For a write operation using write-through protocol during write-hit: The cache location and the main memory location are updated simultaneously.

For a write-miss: For a write-miss, the information is written directly to the main memory

21. What is write-back or copy-back protocol?

For a write operation using this protocol during write-hit: the technique is to update only the cache and to mark it as updated with an associated flag bit, often called the dirty or modified bit. The main memory location of the word is updated later, when the block containing this marked word is to be removed from the cache to make room for a new block.

For a write-miss: the block containing the addressed word is first brought into the cache, and then the deserved word in the cache is overwritten with the new information.

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UNIT V

1. What are the major functions of IO system?

i. Interface to the CPU and memory through the system bus.
ii. Interface to one or more IO devices by tailored data link.

2. What is memory mapped I/O?

When the I/O devices share the same address space, the arrangement is called memory mapped I/O.

3. What is program controlled I/O?

In program controlled I/O the processor repeatedly checks a status flag to achieve the required synchronization between the processor and an input and output device.

4. What is an I/O Interface?

Input-output interface provides a method for transferring binary information between internal storage, such as memory and CPU registers, and external I/O devices

5. Write the factors considered in designing an I/O subsystem?

1. Data Location: Device selection, address of data with in device(track, sector etc)
2. Data transfer: Amount, rate to or from device.
3. Synchronization: Output only when device is ready, input only when data is available.
4. I/O operation: refers to a data transfer between an I/O device and Memory or between an I/O device and CPU.

6. Explain Direct Memory Access.

A modest increase in hardware enables an IO device to transfer a block of information to or from memory without CPU intervention. This task requires the IO device to generate memory addresses and transfer data through the bus using interface controllers.

7. Define DMA controller.

The I/O device interface control circuit that is used for direct memory access is known as DMA controller.

8. What is polling?

Polling is a scheme or an algorithm to identify the devices interrupting the processor. Polling is employed when multiple devices interrupt the processor through one

interrupt pin of the processor.

9. What is the need of interrupt controller?

The interrupt controller is employed to expand the interrupt inputs. It can handle the interrupt requests from various devices and allow one by one to the processor.

10. What are the two independent mechanisms for controlling interrupt request?

At the device end, an interrupt enable bit in a control register determines whether the device is allowed to generate an interrupt request At the processor end, either an interrupt enable nit in the PS or a priority structure determines whether a given interrupt request will be accepted.

11. What is a Priority Interrupt?

A priority interrupt is an interrupt that establishes a priority over the various sources to determine which condition is to be serviced first when two or more requests arrive simultaneously.

12. What are vectored interrupts?

To reduce the time involved in the polling process, a device requesting an interrupt may identify itself directly to the processor. Then the processor can immediately start the executing the corresponding ISR. The schemes based on this approach are called vectored interrupts.

13. Define synchronous bus.

Synchronous buses are the ones in which each item is transferred during a time slot(clock cycle) known to both the source and destination units. Synchronization can be achieved by connecting both units to a common clock source.

14. Define asynchronous bus.

Asynchronous buses are the ones in which each item being transferred is accompanied by a control signal that indicates its presence to the destination unit. The destination can respond with another control signal to acknowledge receipt of the items.

15. What do you mean by memory mapped I/O?

In Memory mapped I/O, there are no specific input or output instructions. The CPU can manipulate I/O data residing in interface registers with the same instructions that are used to manipulate memory words i.e. the same set of instructions are used for reading and writing memory can be used to input and output.

16. What is program-controlled I/O?

In program controlled I/O the processor repeatedly checks a status flags to achieve the required synchronization between the processor and an input and output device.

17. Define interrupt.

An interrupt is any exceptional event that causes a CPUU to temporarily transfer control from its current program to another program , an interrupt handler that services the event in question.

18. What are the different methods used for handling the situation when multiple interrupts occurs?

1) Vectores interrupts
2) Interrupt nesting
3) Simultaneous Requests.

19. What is a privileged instruction?

To protect the operating system of a computer from being corrupted by user programs, certain instructions can be executed only while the processor is in the supervisor mode. These are called privileged instruction.

20. What is bus arbitration?

It is process by which the next device to become the bus master is selected and bus mastership is transferred to it. There are two ways for doing this:

1. Centralized arbitration
2. Distributed arbitration.

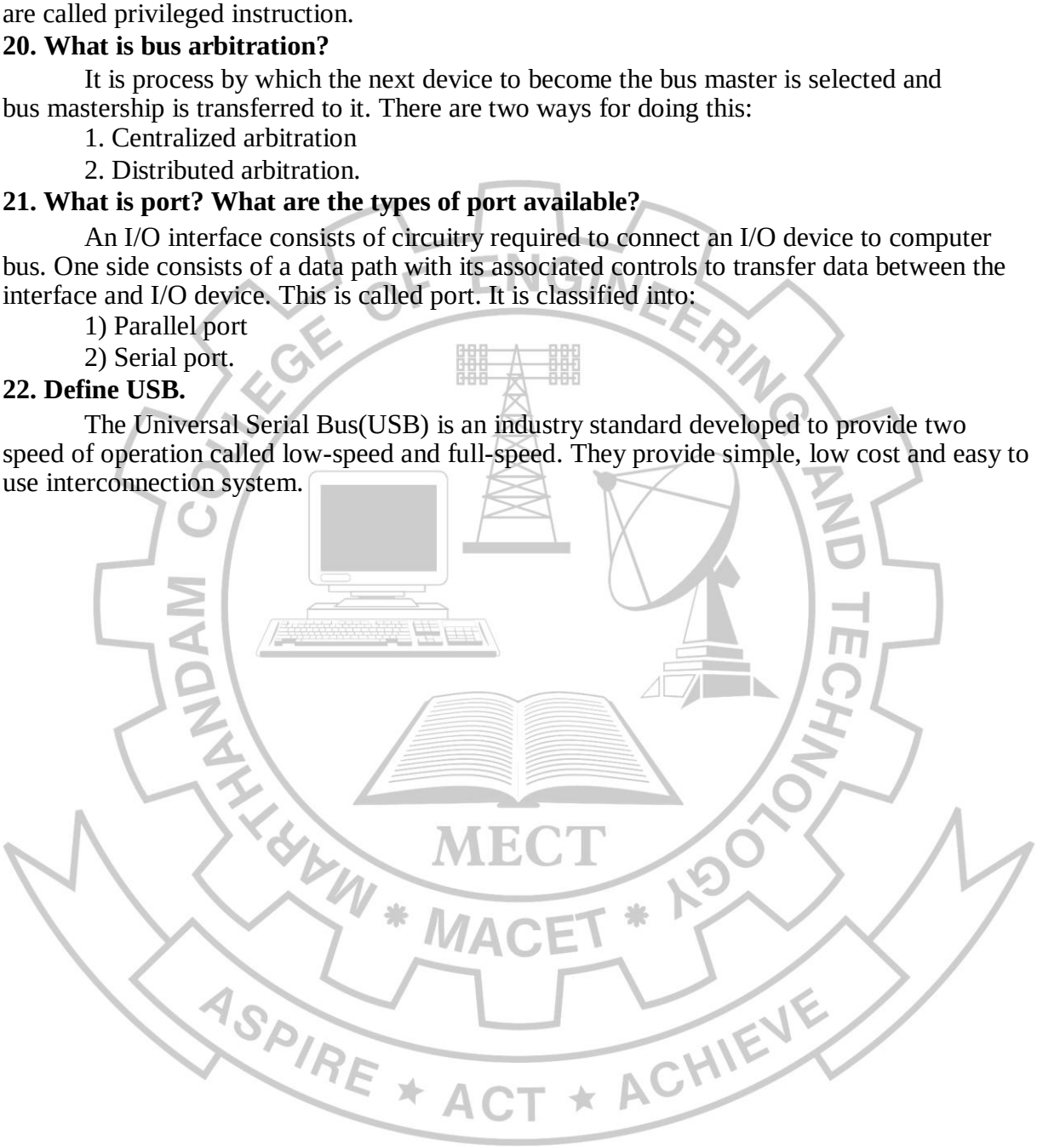
21. What is port? What are the types of port available?

An I/O interface consists of circuitry required to connect an I/O device to computer bus. One side consists of a data path with its associated controls to transfer data between the interface and I/O device. This is called port. It is classified into:

1) Parallel port
2) Serial port.

22. Define USB.

The Universal Serial Bus(USB) is an industry standard developed to provide two speed of operation called low-speed and full-speed. They provide simple, low cost and easy to use interconnection system.



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