

# ANNA UNIVERSITY EXAMINATIONS

## MAY/JUNE 2012 IMPORTANT QUESTIONS

### CS2253 - COMPUTER ORGANISATION AND ARCHITECTURE

#### UNIT I

1. Explain in detail about addressing mode with give an example
2. What are the special registers in a typical computer? Explain their purposes in detail.
3. Explain in detail how Instructions are encoded.
4. Explain the working of a Carry-Look Ahead adder
5. Explain about Instruction Set Architecture with examples

#### UNIT II

1. Explain the basic organization of a micro-programmed control unit and the generation of control signals using micro program
2. Describe the control unit organization with a separate Encoder and Decoder functions in a hardwired control.
3. Explain the basic organization of a microprogrammed control unit and the generation of control signals using micro program.
4. Draw the diagram of the single Bus Organization of the data path inside a processor.

### UNIT III

1. What is instruction hazard? Explain the methods for dealing with the instruction hazards
2. Describe the role of cache memory in pipelined system
3. Explain how the instruction pipeline works. What are the various situations where an instruction pipeline can stall?
4. Discuss the influence of pipelining on instruction set design.
5. What is data hazard? Describe the methods for dealing with the data hazards.

### UNIT IV

1. Explain the different interrupt priority schemes
2. What is a mapping function? What are the ways the cache can be mapped?
3. Explain how the virtual address is converted into real address in a paged virtual memory system.
4. What are the different secondary storage devices? Elaborate on any one of the devices

## UNIT V

1. Explain the following:

- (i) Memory mapped I/O
- (ii) I/O Registers
- (iii) Hardware Interrupts
- (iv) Vectored interrupt

2. Write a note on SCSI BUS. Explain with a neat diagram

3. What are handshaking signals? Explain the handshake control of data transfer during input and output operation.

4. Describe the hardware mechanism for handling multiple interrupt requests.