VELTECH MULTITECH DR.RANGARAJAN DR.SAKUNTHALA ENGINEERING COLLEGE

DEPARTMENT OF CSE

COMPUTER ORGANIZATION AND ARCHITECTURE

CS2253

PREPARED BY:

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VELTECHMULTITECH DR.RANGARAJAN DR.SAKUNTHALA ENGINEERINGCOLLEGE

DEPARTMENT OF COMPUTER SCIENCE

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UNIT I

BASIC STRUCTURE OF COMPUTERS

1. Give the basic performance equation.? (NOV/DEC'2008)

For best performance, it is necessary to design the compiler, machine instruction set and hardware in a co-ordinate way.

Basic Performance Equation:

$$T = (N*S)/R$$

Where, T-Performance Parameter

R→Clock Rate in cycles/sec

N→-Actual number of instruction execution

S→-Average number of basic steps needed to execute one machine instruction. To achieve high performance,

2. What is a bus ?what are the different buses in the CPU?(NOV/DEC'2006)

A group of lines that serves as the connection path to several devices is called a Bus. A Bus may be lines or wires or one bit per line.

The lines carry data or address or control signal

There are 2 types of Bus structures. They are

- Single Bus Structure
- Multiple Bus Structure

3 .Give the different types of addressing modes? (NOV/DEC'2007)

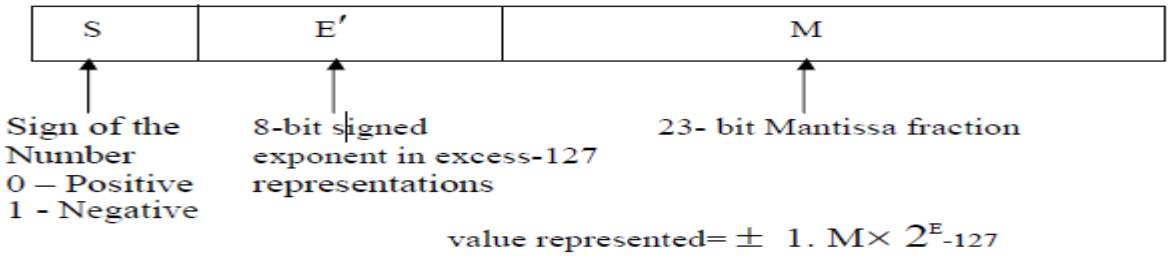
The various addressing modes are

1.Absolute addressing mode
2.Register addressing mode
3.Indirect addressing mode
4.Index addressing mode
5.Immediate addressing mode
6.Relative addressing mode
7.Autoincrement addressing mode
8.Autodecrement addressing mode

4. Difference between RISC AND CISC processor?(April/May'2010)

	CISC	RISC
1	Complex instructions taking multiple cycles	Simple instructions taking 1 cycle
2	Any instruction may reference memory	Only LOADS/STORES reference memory
3	Not pipelined or less pipelined	Highly piplined
4	Instructions interpreted by the microprogram	Instructions executed by the hardware
5	Variable format instructions	Fixed format instructions
6	Many instructions and modes	Few instructions and modes
7	Complexity in the microprogram	Complexity is in the compiler
8	Single register set	Multiple register sets

5. Give the IEEE standard for floating point numbers for single precision number? ?(NOV/DEC'2007)



value represented= $\pm$ 1. M$\times$ 2^{E-127}

6. Define SPEC rating?(MAY/JUNE 2009)

A non-profit organization called SPEC(System Performance Evaluation Corporation) selects and publishes representative application program

$$\text{SPEC rating} = \frac{\text{Running time on reference computer}}{\text{Running time on computer under test}}$$

The Overall SPEC rating for the computer is given by,

$$\text{SPEC rating} = \left(\prod_{i=1}^{n} \text{SPECi} \right)^{1/n}$$

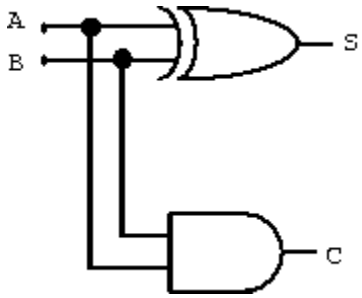
7. Difference between auto increment and auto decrement addressing mode(April/May'2010)

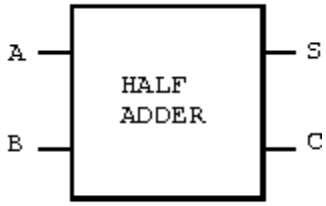
Autoincrement Mode = after operand addressing , the contents of the register is incremented.

AutoDecrement Mode = before operand addressing, the contents of the register is decrement.

8. Write the logical equation of binary half adder (April/May'2011)

A half adder is a logic circuit with two inputs and two outputs, which adds two bits at a time, producing a sum and a carry.





9. Define word length/(NOV/DEC'2011)

Word is a term for the natural unit of data used by a particular processor design. A word is basically a fixed sized group of bits that are handled as a unit by the instruction set and/or hardware of the processor. The number of bits in a word (the word size, word width, or word length) is an important characteristic of a specific processor design or computer architecture.

10. Define overflow and underflow?(MAY/JUNE'2008/2009)

Mantissa overflow

The addition of two mantissa of the same sign may result in a carry of th most significant bit If so, the mantissa is shifted right ad the exponent is incremented

Mantissa underflow

The digits may flow off the right end of the mantisa. In such case truncation methods such as chopping, rounding are used.

16 MARKS

1. **Write notes on Instruction formats. (NOV/DEC 2007) &(APRIL/MAY 2008)**

   Basic instruction types

   - zero address instruction
   - One address instruction
   - Two address instruction
   - Three address instruction

   A computer must have instruction capable of performing the following operations.

   They are

   - Data transfer between memory and processor register.
   - Arithmetic and logical operations on data.
   - Program sequencing and control.
   - I/O transfer.

2. Explain about Instruction & Instruction Sequencing? (NOV/DEC 2006)

INSTRUCTION AND INSTRUCTION SEQUENCING

A computer must have instruction capable of performing the following operations. They are,

- Data transfer between memory and processor register.
- Arithmetic and logical operations on data.
- Program sequencing and control.
- I/O transfer.

Instruction Execution and Straight–line Sequencing:
Instruction Execution:

- The Instruction Fetch
- Instruction Execution

3. Explain about Addressing modes?(NOV/DEC 2007) & (NOV/DEC 2006) & (MAY/JUNE 2007)

ADDRESSING MODES

The different ways in which the location of an operand is specified in an instruction is called as Addressing mode.

Generic Addressing Modes:

- Immediate mode
- Register mode
- Absolute mode
- Indirect mode
- Index mode
- Base with index
- Base with index and offset
- Relative mode
- Auto-increment mode
- Auto-decrement mode

4. Design a 4-bit Carry-Look ahead Adder and explain its operation with an example. (APRIL/MAY 2008) & (NOV/DEC 2007)

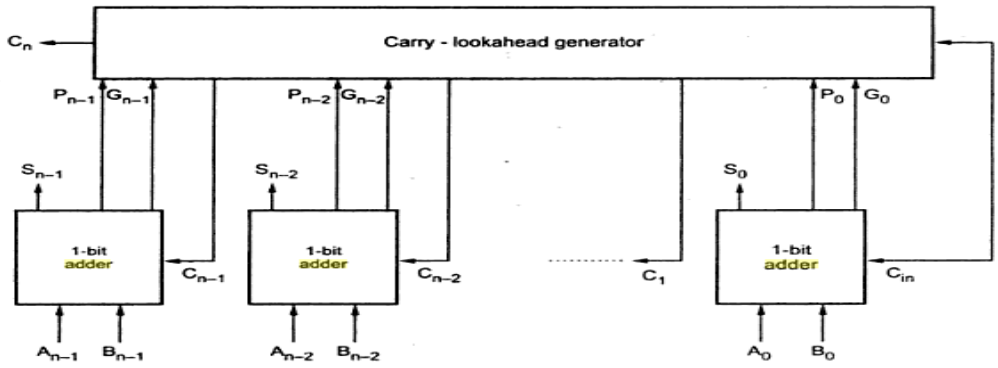


Fig. 2.9 General form of a carry-lookahead adder circuit

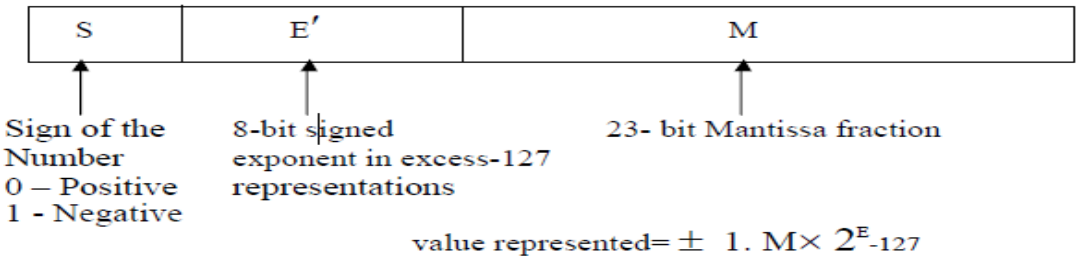
Functions

Carry generate $G_i = A_i.B_i$
Carry propagate $Pi = (A_i$ Å $B_i)$

$C_1 = G_0 + P_0.C_0$
$C_2 = G_1 + P_1.C_1 = G_1 + P1.G_0 + P_1.P_0.C_0$
$C_3 = G_2 + P_2.G_1 + P_2.P_1.G_0 + P_2.P_1.P_0.C_0$
$C_4 = G_3 + P_3.G_2 + P_3.P_2.G_1 + P_3P_2.P_1.G_0 + P_3P_2.P_1.P_0.C_0$

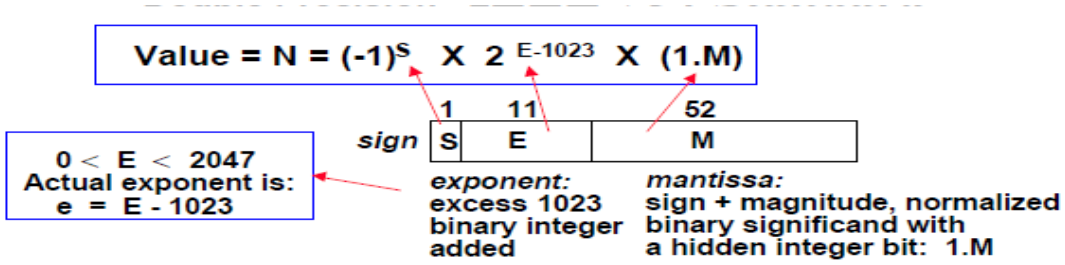
5.. Give the IEEE standard single and double precision floating point format.(NOV/DEC 2006)

Single precision floating point format



Brief explanation

Double Precision Floating Point Format- diagram



Brief explanation

UNIT-II

2-marks

1.what are the sequence of operations involved in processing an instruction constitutes an instruction cycle? MAY/JUNE'2006)

The sequence of operations involved in processing an instruction constitutes an instruction cycle,which can be subdivided into 3 major phases:

1. Fetch cycle
2. Decode cycle
3. Execute cycle

2. Difference between hardwired control and Microprogrammed control(MAY/JUNE'2007)

Attribute	**Hardwired Control**	**Microprogrammed Control**
Speed	Fast	Slow
Control functions	Implemented in hardware	Implemented in software
Flexibility	Not flexible to accommodate new system specifications or new instructions	More flexible, to accommodate new system specification or new instructions redesign is required
Ability to handle large/complex instruction sets	Difficult	Easier
Ability to support operating systems	Very difficult	Easy

3.Comparison between horizontal and vertical organization(april/may'2010)

S.No	**Horizontal**	**Vertical**
1	Long formats	Short formats
2	Ability to express a high degree of parallelism	Limited ability to express parallel microoperations
3	Little encoding of the control information	Considerable encoding of the control information
4	Useful when higher operating speed is desired	Slower operating speeds

4. Define hardwired control. (Nov/Dec'2003)

Hard-wired control can be defined as sequential logic circuit that generates specific sequences of control signal in response to externally supplied instruction.

5. Define microprogrammed control. (May/June'2008)

A microprogrammed control unit is built around a storage unit is called a control store, where all the control signals are stored in a RAM or RAM called a control memory. The control signal to be activate dat any time are specified by a micro instruction.

6. What are advantage and disadvantage of hardwired control and Microprogrammed control(MAY/JUNE'2007)

Advantages of Microprogrammed control

- It simplifies the design of control unit. Thus it is both, cheaper and less error phrone implement.
- Control functions are implemented in software rather than hardware.

Disadvantages

- A microprogrammed control unit is somewhat slower than the hardwired control unit, because time is required to access the microinstructions from CM.
- The flexibility is achieved at some extra hardware cost due to the control memory and its access circuitry.

7. What are the address sequencing capabilities required in control memory? (Nov/Dec'2006)

Each microinstruction should explicitly or implicitly specify the next micro instruction to be used, such address sequencing capabilities are required in the control memory

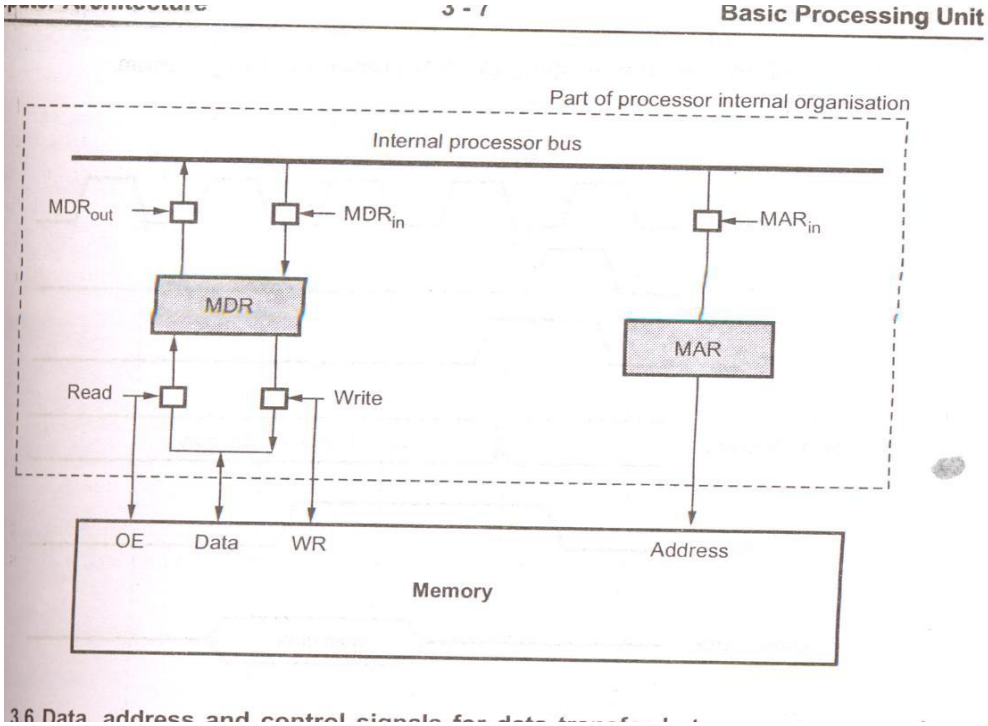
8. What is microprogram? (NOV/DEC 2009)

A sequence of one or more micro operation designed to control specific operation such as addition ,multiplication is called a micro program

9. Define microinstruction? (APRIL/MAY 2003)

The control signal to be activated at any time are specified by a microinstruction

10. Draw the connection between main memory andn CPU(Nov/Dec'2007)



3.6 Data, address and control signals for data transfer

16 marks

1. **Define bus and draw the structure of Multiple Bus Organisation(May/June 2007)**

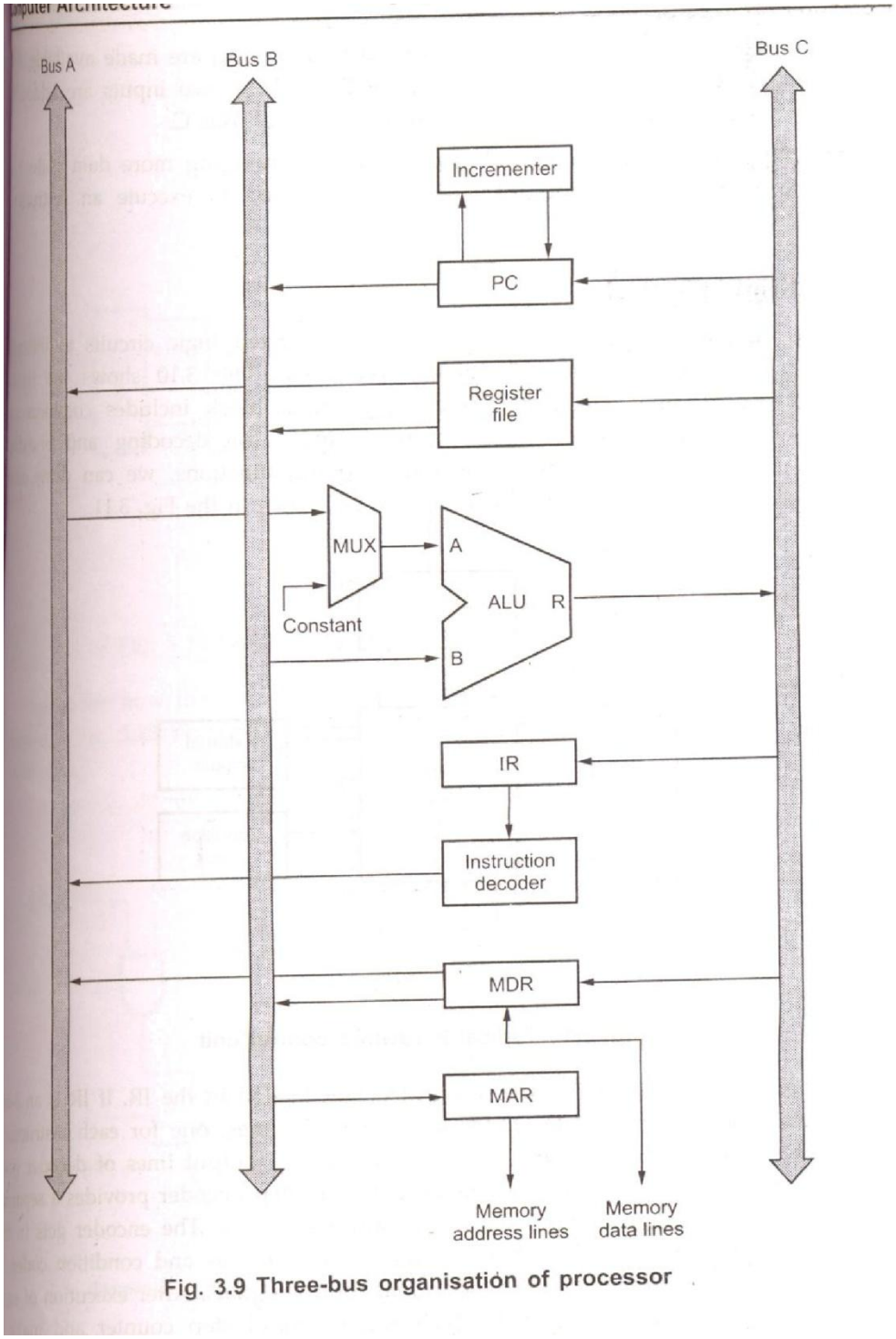


Fig. 3.9 Three-bus organisation of processor

Three bus organization control bus operating steps

2. Explain the Organization of Hardwired control in detail. (NOV/DEC 2006)

The control units use fixed logic circuits to interpret instructions and generate control signals from them.

The fixed logic circuit block includes combinational circuit that generates the required control outputs for decoding and encoding functions

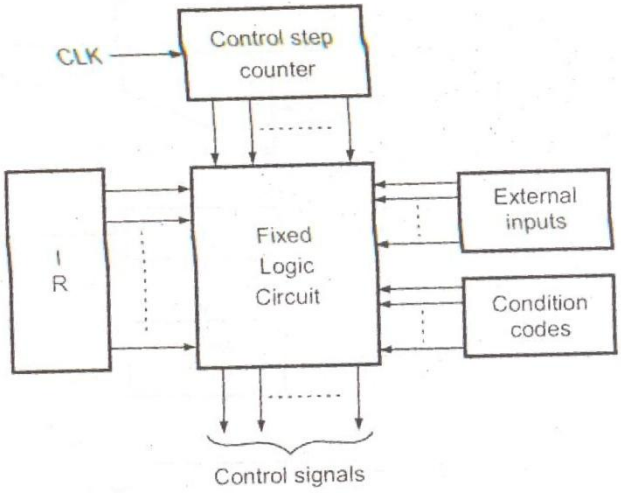


Fig. 3.10 Typical hardwired control unit

decoder decodes the instruction loaded in the IF

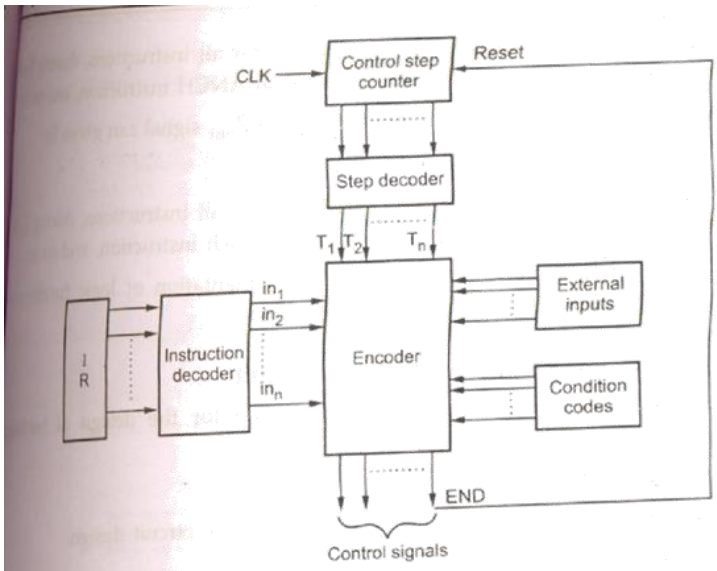
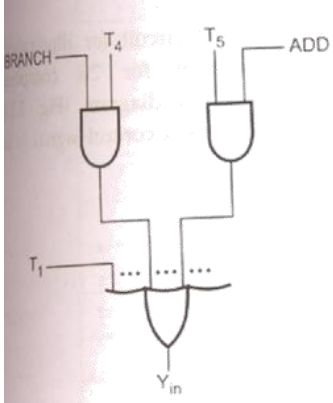


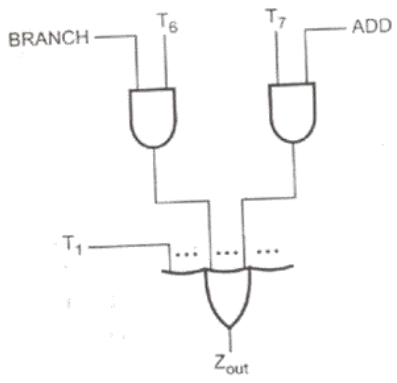
Fig. 3.11 Detail block diagram for hardwired control unit

Let us see how the encoder generates signal for single bus processor organisation wn in Fig. 3.12 Y_{in}. The encoder circuit implements the following logic function to erate Y_{in}.

$$Y_{in} = T_1 + T_5 \cdot ADD + T_4 \cdot BRANCH + \ldots$$



Generation of the Y_{in} control signal



Generation of the Z_{out} control signal

Instruction decoder

Step decoder

Encoder

The encoder circuit implements the following logic function to generate Y_{in}

$Y_{in} = T_1 + T_5$. Add + T . BRANCH+…

The Y_{in} signal is asserted during time interval T_1 for all instructions, during T_5 for an ADD instruction, during T_4 for an unconditional branch instruction, and so on.

As another example, the logic function to generate Z_{out} signal can given by

$Z_{out} = T_2 + T_7$. ADD + T_6 . BRANCH +….

The Z_{out} signal is asserted during time interval T_2 of all instructions, during T_7 for an ADD instruction, during T_6 for an unconditional branch instruction, and so on.

A Complete processor

Instruction unit- It fetches instructions from an instruction cache or from the main memory when the desired instructions are not available in the cache.

Integer unit – To process integer data

Floating unit – To process floating –point data

Data cache – The integer and floating unit gets data from data cache

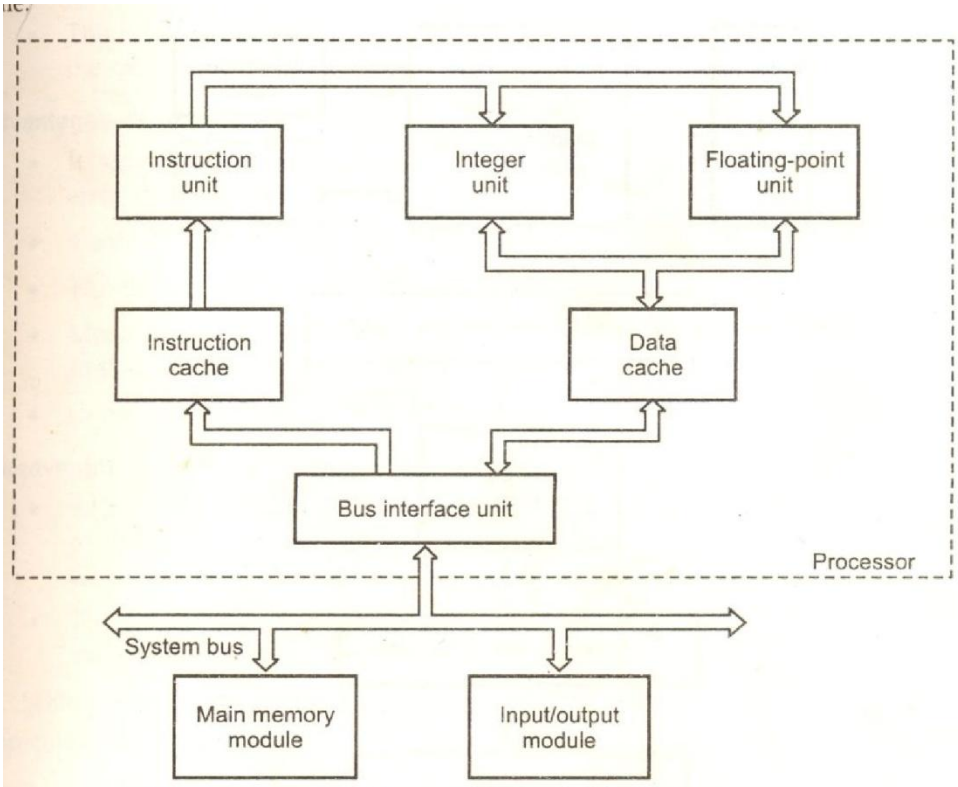


Fig. 3.14 Block diagram of a complete processor

3. Explain the Organization of Micro programmed control unit in detail.(NOV/DEC 2007) & (MAY/JUNE 2006) & (NOV/DEC 2006)

Operating steps

- Every instruction in a processor is implemented by a sequence of one or more sets of concurrent micro operations.
- Each micro operation is associated with a specific set of control lines which, when activated, causes that micro operation to take

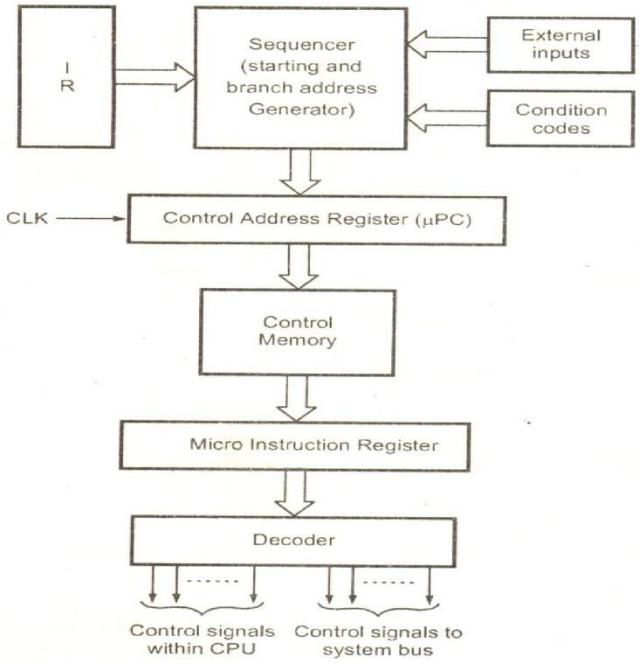


Fig. 3.15 Microprogrammed control unit

The microprogrammed control unit,

- control memory
- control address register
- micro instruction register
- microprogram sequencer

Advantages of Microprogrammed control

- It simplifies the design of control unit. Thus it is both, cheaper and less error phrone implement.
- Control functions are implemented in software rather than hardware.
- The design process is orderly and systematic
- More flexible, can be changed to accommodate new system specifications or to correct the design errors quickly and cheaply.
- control unit, because time is required to access the microinstructions from CM.
- The flexibility is achieved at some extra hardware cost due to the control memory and its access circuitry.

Microinstruction

A simple way to structure microinstructions is to assign one bit position to each control signal required in the CPU.

Grouping of control signals

Grouping technique is used to reduce the number of bits in the microinstruction. Gating signals: IN and OUT signals

Control signals: Read,Write, clear A, Set carry in, continue operation, end, etc. ALU signals: Add, Sub,etc;

There are 46 signals and hence each microinstruction will have 46 bits.

It is not at all necessary to use all 46 bits for every microinstruction because by using grouping of control signals we minimize number of bits for microinstruction

Way to reduce number of bits microinstruction:

- Most signals are not needed simultaneously. Many signals are mutually exclusive
- e.g. only one function of ALU can be activated at a time.

Vertical organisation

Highly encoded scheme that can be compact codes to specify only a small number of control functions in each microinstruction are referred to as a vertical organisation.

Horizontal organisation

The minimally encoded scheme, in which resources can be controlled with a single instruction is called a horizontal organisation.

Advantages of vertical and horizontal organization

1. Vertical approach is the significant factor,it is used to reduce the requirement for the parallel hardware required to handle the execution of microinstructions.
2. Less bits are required in the microinstruction.
3. The horizontal organisation approach is suitable when operating speed of computer is a critical factor and where the machine structure allows parallel usage of a number of resources.

Disadvantages

Vertical approach results in slower operations speed.

Microprogram sequencing

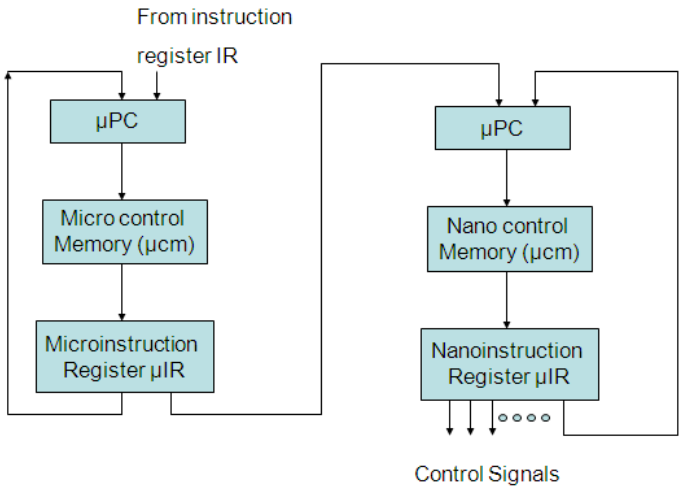
The task of microprogram sequencing is done by microprogram sequencer. 2 important factors must be considered while designing the microprogram sequencer:

4.Difference between hardwired control and Microprogrammed control.(MAY/JUNE 2007)

Attribute	Hardwired Control	Microprogrammed Control
Speed	Fast	Slow
Control functions	Implemented in hardware	Implemented in software
Flexibility	Not flexible to accommodate new system specifications or new instructions	More flexible, to accommodate new system specification or new instructions redesign is required
Ability to handle large/complex instruction sets	Difficult	Easier
Ability to support operating systems	Very difficult	Easy
Design process	Complicated	Orderly and systematic
Applications	Mostly RISC microprocessors	Mainframes, some microprocessors
Instructionset size	Usually under 100 instructions	Usually over 100 instructions
ROM size	-	2K to 10K by 20-400 bit microinstructions
Chip area efficiency	Uses least area	Uses more area

5.Write short notes on Nanoprogramming and draw the structure of nanoinstruction sequencing organization/. (APRIL/MAY 2008)

- Definition
- Advantages of nanoprogramming
- Disadvantages of nanoprogramming
- Diagram-Nanoinstruction sequencing organization



Two Level control store organization for nano programming

UNIT-III

PIPELINING

1. **State different types of hazards that occur in pipeline?(April/May'2003) (Nov/Dec'2004)**

The various pipeline hazards are:

1. Data hazard
2. Structural Hazard
3. Control Hazard

2. **What are the two types of branch prediction technique available? (**MAY/JUNE2009)_

The two types of branch prediction techniques are

1) Static branch prediction
2) Dynamic branch prediction

3. Define pipelining.?(April/May'2003)

Pipelining is an effective way of organizing concurrent activity in a computer system. The processor executes the program by fetching and executing instructions, one after the other.

4. Name the four stages of pipelining.?(NOV/DEC2007)

Fetch: read the instruction from the memory.
Decode: decode the instruction and fetch the source operand.
Execute: perform the operation specified by the instruction.
Write: store the result in the destination location.

5.Define Register renaming?(NOV/DEC2009)

When temporary register holds the contents of the permanent register, the name of permanent register is given to that temporary register is called as register renaming.

For example, if I2 uses R4 as a destination register, then the temporary register used in step TW2 is also reffered as R4 during cycles 6 and 7, that temporary register used only for instructions that follow I2 in program order.

For example, if I1 needs to read R4 in cycle 6 or 7, it has to access R4 though it contains unmodified data be I2.

6. What is structural hazard?(NOV/DEC2008)

The hazard are because of resource conflicts due to insufficient resource,when even with all possible combination,it may not be possible to overlap the operation

7. **What is data hazard in pipelining?(NOV/DEC 2007/2008)**

Arise when an instruction depends on the results of a previous instruction in a way that is exposed by overlapping of instruction in pipeline

Types

- RAW
- WAW
- WAR

8. **What is pipelining? What are the advantages of pipelining?(APRIL/MAY2010)**

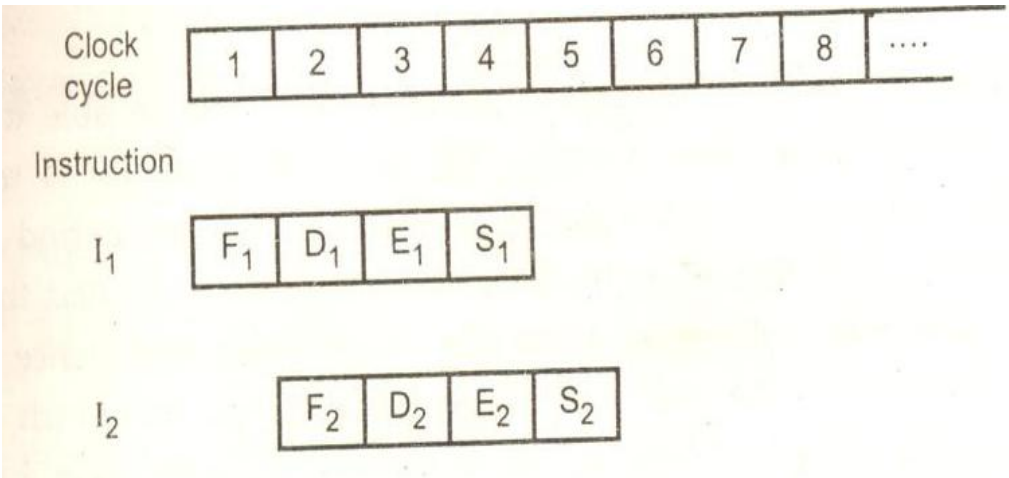
- Pipelining is an effective way of organizing concurrent activity in a computer system. The processor executes the program by fetching and executing instructions, one after the other.
- ***Pipeline Hazards*** are situations that prevent the next instruction in the instruction stream from executing in its designated clock cycle
- Hazards reduce the performance from the ideal speedup gained by pipelining

9. **Distinguish between static and dynamic branch prediction(MAY/JUNE2009)**

STATIC BRANCH PREDICTION	DYNAMIC BRANCH PREDICTION
Branch can be predicted based on branch codes type statistically	It used recent branch history during program execution,information is stored in buffer called branch target buffer(BTB)
It may not produce accurate result every time	Processing of conditional branches with zero delay

10. **Draw the structure of two stage pipelining(NOV/DEC 2007)**

Fetch: read the instruction from the memory.
Decode: decode the instruction and fetch the source operand.
Execute: perform the operation specified by the instruction.
Write: store the result in the destination location.



16 mark

1. **Define pipelining and explain in detail about the data hazard concepts?(NOV/DEC'08)**

Basic Concepts

Stages of pipelining

F Fetch: read the instruction from the memory
D Decode: decode the instruction and fetch the source operand(s)
E Execute: perform the operation specified by the instruction
W Write: store the result in the destination location

Pipelined execution

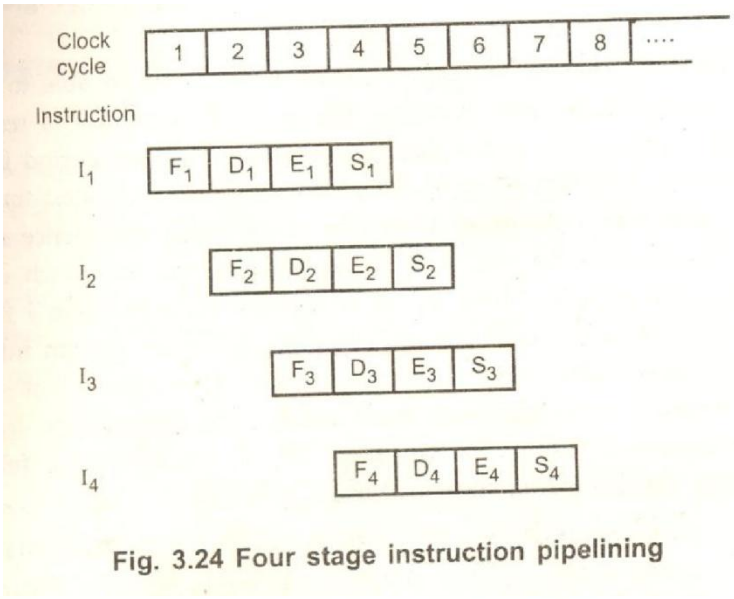


Fig. 3.24 Four stage instruction pipelining

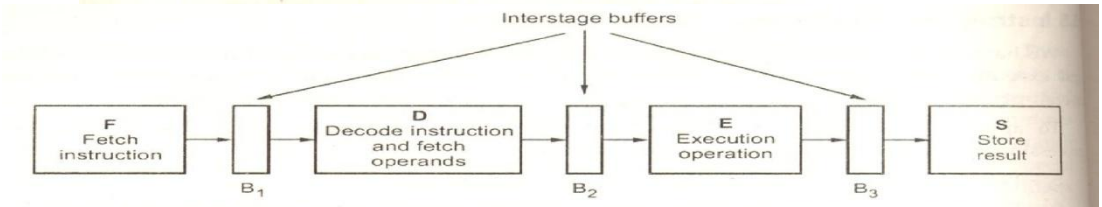


Fig. 3.25 Hardware organisation for four-stage instruction pipeline

3.8.1 Hazards in Instruction Pipelining

Pipeline performance

Pipelining is proportional to the number of pipeline stages.

For variety of reasons, one of the pipeline stages may not be able to complete its processing task for a given instruction in the time allotted.

For eg, stage E in the four-stage pipeline is responsible for arithmetic and logic operations and one clock cycle is assigned for this task.

Types

- RAW
- WAR

2. Explain the various types of hazards and solution to overcome?(NOV/DEC '09)

Contents to be covered

- DEFINITION

Types of hazard

- Data hazard
- Control hazard
- Structural hazard

Pipeline Hazards are situations that prevent the next instruction in the instruction stream from executing in its designated clock cycle

Hazards reduce the performance from the ideal speedup gained by pipelining

Three types of hazards

Structural hazards

Arise from resource conflicts when the hardware can't support all possible combinations of overlapping instructions

Data hazards

Arise when an instruction depends on the results of a previous instruction in a way that is exposed by overlapping of instruction in pipeline

Control hazards

Arise from the pipelining of branches and other instructions that change the PC (Program Counter)

3. Design a four stage instruction pipeline show its performance is improved over sequential execution? ?(NOV/DEC '07)

Stages of pipelining

Performance consideration

Effects of instruction hazard

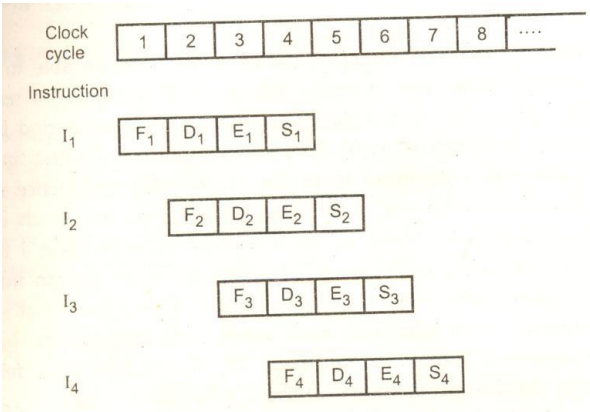


Fig. 3.24 Four stage instruction pipelining

4.Explain how pipeline helps to speed up the processor, discuss the hazard that have to be taken care of in a pipelined processor?(MAY/JUNE 2006)

Stages of pipelining

Fetch: read the instruction from the memory
Decode: decode the instruction and fetch the source operand(s)
Execute: perform the operation specified by the instruction
Write: store the result in the destination location

To apply the concept of instruction pipelining,the instruction process is divided in to four stages with the subdivision and assuming equal duration for each stage ,we can reduce the execution time for 4 instruction from 16 time units

- Types of hazard
  - Data hazard
  - Control hazard
  - Structural hazard

Pipeline Hazards are situations that prevent the next instruction in the instruction stream from executing in its designated clock cycle

Hazards reduce the performance from the ideal speedup gained by pipelining

4. Discuss the data and control path method in pipelining? ?(NO/DEC 2011)

Datapath and control considerations

When single bus is used in a processor only one data word can be transferred over the bus in a clock cycle. This increases the steps required to complete the execution of the instruction. To reduce the number of steps needed to execute instructions most commercial processors provide multiple internal paths that enable several transfer to take place in parallel.

Modified 3 bus structure of the processor for pipelined execution

3 buses are used to connect registers and the ALU of the processor.

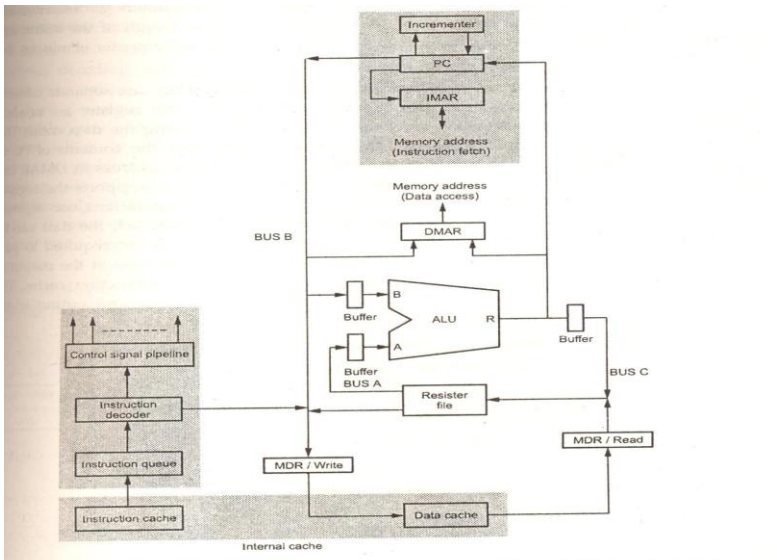


Fig. 3.31 Modified three-bus structure of the processor for pipelined execution

UNIT IV

MEMORY SYSTEM

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1. Give the features of a ROM cell (APRIL/MAY 2008)

Memories whose content cannot be altered online if they can be altered at all are read only memories.

Features:

- It is a non volatile memory
- Accessed randomly with unique addresss

2. List the differences between static RAM and dynamic RAM.(APRIL/MAY 2008)

Static RAM	Dynamic RAM
Less memory space per unit area	More memory cells
Less access time	Access time is greater
Refreshing circuitry is not required	Refreshing circuitry is required
Cost is more	Cost is less

3. Define Locality of Reference. (NOV/DEC 2009)&(APRIL/ MAY 2008)

The point is that many instruction in localized area of the program are executed repeatedly during some time time period and the remainder of the program is accessed in frequently

Types:

Temproral

Spatial

4. What is Translation Look aside Buffer? (MAY/JUNE 2006)

- The Page table is placed in the main memory but a copy of the small portion of the page table is located within MMU.
- This small portion or small cache is called Translation **LookAside Buffer(TLB).**

5. What is memory interleaving? (NOV/DEC'10)

The memory access time is a bottle neck in the system. One way to reduce it is to use cache memory. Alternative technique to reduce memory access time is called memory inter leaving

6. Discuss the different mapping techniques used in cache memory(NOV/DEC2002)

- **Direct mapping**
- **Associative mapping**
- **Two way set associative mapping**

7. Define hit ratio(NOV/DEC2006)

Hit rate=No of hits/no of bus cycles *100%

8. What is virtual memory(MAY/JUNE 2009)

Techniques that automatically move program and data blocks into the physical main memory when they are required for execution is called the **Virtual Memory.**

9.what are the types of memory(May/June 2009)

- Static RAM memory
- Dynamic RAM memory

10.what is data stripping?(NOV/DEC2009)

In a write system a single large file is stored in several separate disk units by breaking the file up in to a number of small pieces and stored these pieces on different disk

16 MARKS

1. Explain about Static & Dynamic memory systems. (NOV/DEC 2007)

SEMI CONDUCTOR RAM MEMORIES:

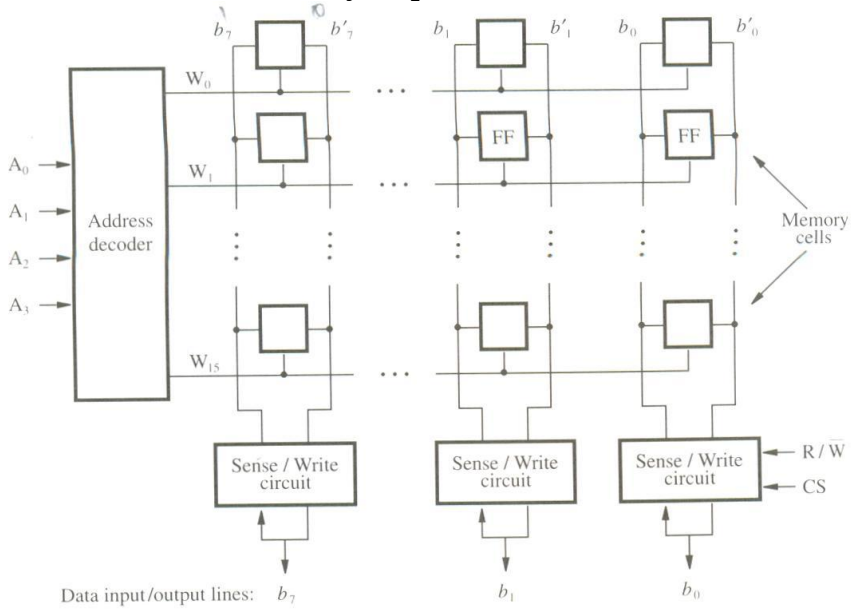
Semi-Conductor memories are available is a wide range of speeds.

INTERNAL ORGANIZATION OF MEMORY CHIPS:

Memory cells are usually organized in the form of array, in which each cell is capable of storing one bit of in formation.

Each row of cells constitute a memory word and all cells of a row are connected to a common line called as **word line**.

Fig: Organization of bit cells in a memory chip



static Memories:

Memories that consists of circuits capable of retaining their state as long as power is applied are known as **static memory.**

Fig:Static RAM cell

Read Operation:

Write Operation:

Fig:CMOS cell (Complementary

Demerit:

SRAM‟s are said to be volatile memories because their contents are lost when the power is interrupted.

Asynchronous DRAMS:-

- Less expensive RAM‟s can be implemented if simplex calls are used such cells cannot retain their state indefinitely. Hence they are called **Dynamic RAM's (DRAM).**

2.Explain about Cache memory in detail with mapping function. (NOV/DEC 2006)

CACHE MEMORIES

The effectiveness of cache mechanism is based on the property of „**Locality of reference'.**

Locality of Reference:

Many instructions in the localized areas of the program are executed repeatedly during some time period and remainder of the program is accessed relatively infrequently.

It manifests itself in 2 ways.They are,

- **Temporal**(The recently executed instruction are likely to be executed again very soon.)
- **Spatial(**The instructions in close proximity to recently executed instruction are also likely to be executed soon.)

If the active segment of the program is placed in cache memory, then the total execution time can be reduced significantly.

The collection of rule for making this decision is called the **replacement algorithm.**

In a Read operation, the memory will not involve.

The write operation is proceed in 2 ways.They are,

- Write-through protocol
- Write-back protocol

Write-through protocol:

Here the cache location and the main memory locations are updated simultaneously.

Write-back protocol:

This technique is to update only the cache location and to mark it as with associated flag bit called **dirty/modified bit.**

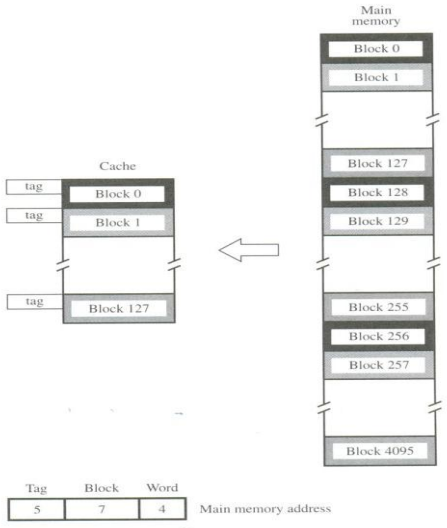
R**ead Miss:** The block of words that contains the requested word is copied from the main memory into cache.

If the requested word not exists in the cache during write operation,then **Write Miss** will occur.

Mapping Function:

Direct Mapping:

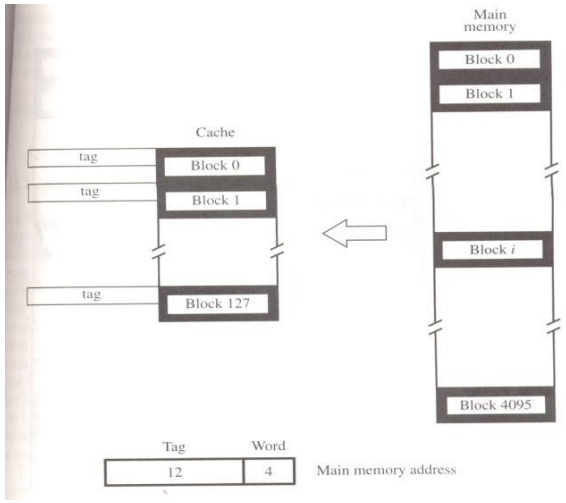
Fig: Direct Mapped Cache



Merit:
It is easy to implement.
Demerit:
It is not very flexible.

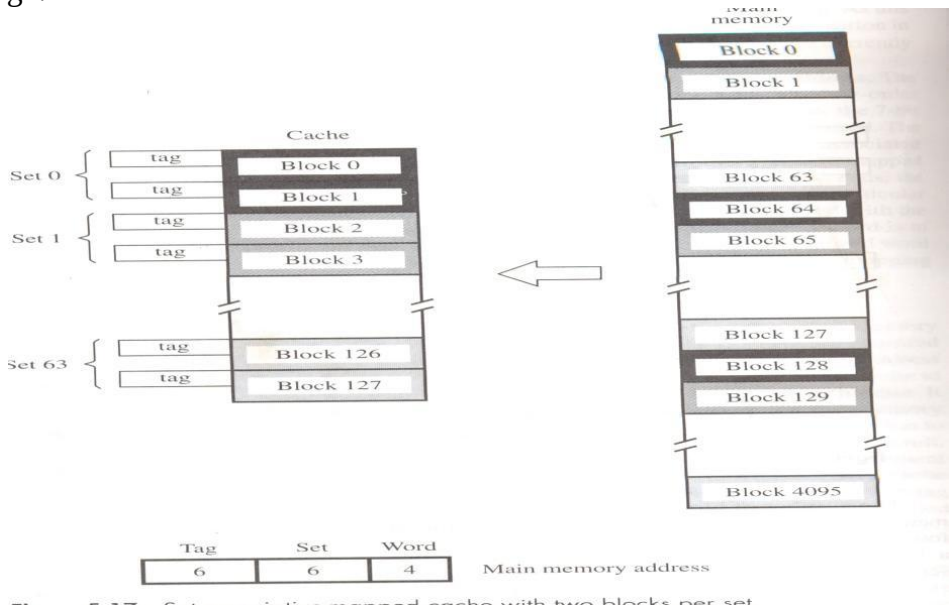
Associative Mapping:

In this method, the main memory block can be placed into any cache block position.



Merit:
It is more flexible than direct mapping technique.

Demerit:
Its cost is high.



Set-Associative Mapping:

- It is the combination of direct and associative mapping.

3. Explain how the virtual address is converted into real address in a paged virtual memory system. (APRIL/MAY 2008)

VIRTUAL MEMORY:

Techniques that automatically move program and data blocks into the physical main memory when they are required for execution is called the **Virtual Memory.**

The binary address that the processor issues either for instruction or data are called the **virtual / Logical address**.

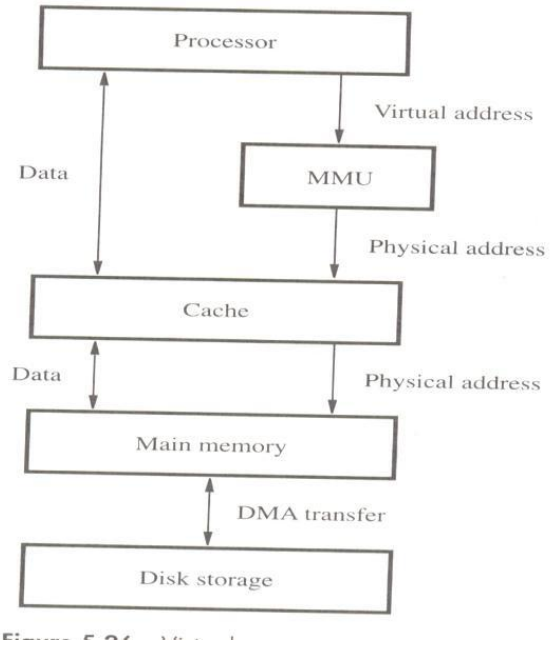
The virtual address is translated into physical address by a combination of hardware and software components.This kind of address translation is done by **MMU**(Memory Management Unit).

When the desired data are in the main memory ,these data are fetched /accessed immediately.

If the data are not in the main memory,the MMU causes the Operating system to bring the data into memory from the disk.

Virtual Memory Organisation

Address Translation:



Address Translation:

In address translation,all programs and data are composed of fixed length units called **Pages.**

The Page consists of a block of words that occupy contiguous locations in the main memory.

The pages are commonly range from 2K to 16K bytes in length.

The **cache bridge** speed up the gap between main memory and secondary storage and it is implemented in software techniques.

Each virtual address generated by the processor contains **virtual Page number**(Low order bit) and **offset**(High order bit)

Virtual Page number+ Offset Specifies the location of a particular byte (or word) within a page.

Page Table:

It contains the information about the main memory address where the page is stored & the current status of the page.

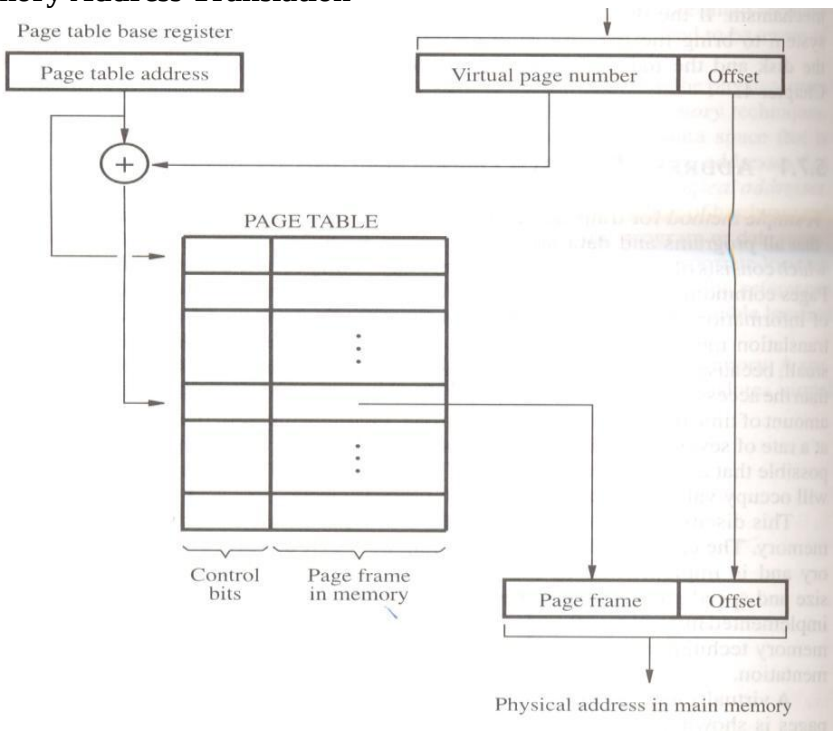
Page Frame:
An area in the main memory that holds one page is called the page frame.

Function:

The control bit indicates the validity of the page ie)it checks whether the page is actually loaded in the main memory.

It also indicates that whether the page has been modified during its residency in the memory;this information is needed to determine whether the page should be written back to the disk before it is removed from the main memory to make room for another page.

Fig:Virtual Memory Address Translation



- The Page table information is used by MMU for every read & write access.
- The Page table is placed in the main memory but a copy of the small portion of the page table is located within MMU.
- This small portion or small cache is called Translation **LookAside Buffer(TLB).**
- This portion consists of the page table enteries that corresponds to the most recently accessed pages and also contains the virtual address of the entry

4. Discuss the address translation mechanism and the different page replacement policies used in a virtual memory system. (MAY/JUNE 2006)

- Virutual memory definition
- Virtual memory organisation
- Address translation mechanism
- Page replacement policies

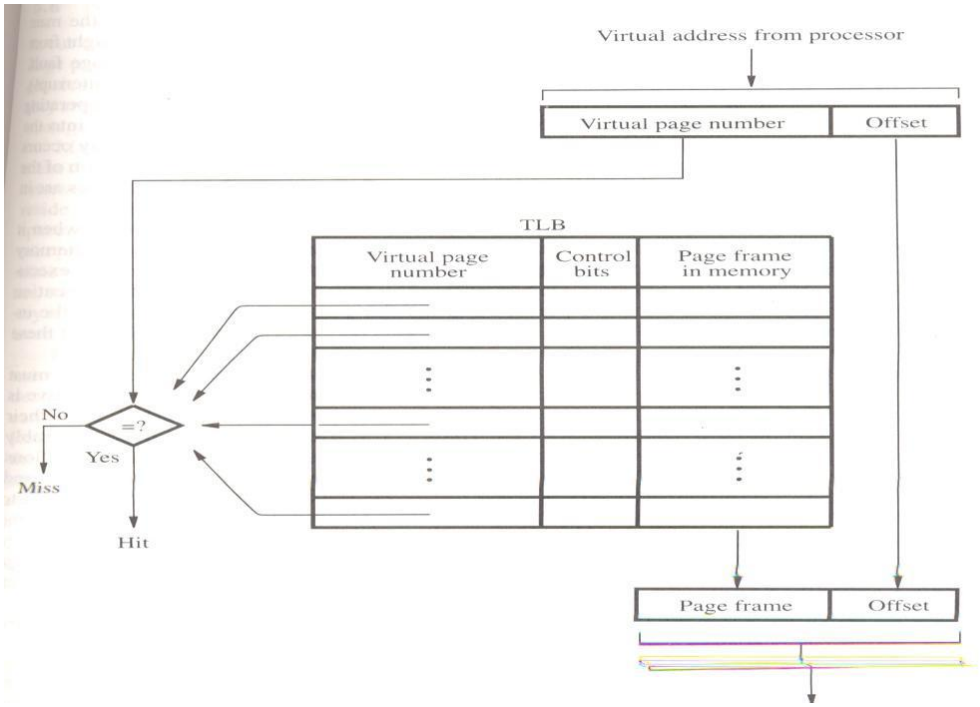
FIFO-FIRST IN FIRST OUT
LRU-LEAST RECENTLY USED
LFU-LEAST FREQUENTLY USED
RU-RANDOMLY USED

5.How a virtual address gets translated into a physical address? Explain in detail with a neat diagram. Explain the use of TLB.(APRIL/MAY 2008)&(NOV/DEC 2006) & (MAY/JUNE 2007)

DIAGRAM -virtual address g translation into a physical address

Translation methods
Address translation methods
Segment translation methods
Page translation methods

Fig-Translation methods-translation look aside buffer



When the operating system changes the contents of page table ,the control bit in TLB will invalidate the corresponding entry in the TLB.

Given a virtual address,the MMU looks in TLB for the referenced page.

If the page table entry for this page is found in TLB,the physical address is obtained immediately.

If there is a miss in TLB,then the required entry is obtained from the page table in the main memory & TLB is updated.

When a program generates an access request to a page that is not in the main memory ,then Page Fault will occur.

The whole page must be broght from disk into memry before an access can proceed.

When it detects a page fault,the MMU asks the operating system to generate an interrupt.

The operating System suspend the execution of the task that caused the page fault and begin execution of another task whose pages are in main memory because the long delay occurs while page transfer takes place.

UNIT V

I/O ORGANIZATION

1.What is meant by bus arbitration?(APRIL/MAY'2010)

It is the process by which the next device to become the bus master is selected and the bus mastership is transferred to it.

Types:

There are 2 approaches to bus arbitration. They are,

- Centralized arbitration (A single bus arbiter performs arbitration)
- Distributed arbitration (all devices participate in the selection of next bus master).

2. Name and give purpose of widely used bus standards? APRIL/MAY'2010)

- Asynchronous bus
- Synchronous bus

3.What is distributed arbitration?(APRIL/MAY'2011)

Distributed Arbitration:

It means that all devices waiting to use the bus have equal responsibility in carrying out the arbitration process.

4.What is interrupt (MAY/JUNE2009)

When a program enters a wait loop, it will repeatedly check the device status. During this period, the processor will not perform any function.

The Interrupt request line will send a hardware signal called the interrupt signal to the processor.

On receiving this signal, the processor will perform the useful function during the waiting period.

5.Define DMA?(MAY/JUNE2009)

A special control unit may be provided to allow the transfer of large block of data at high speed directly between the external device and main memory , without continous intervention by the processor. This approach is called **DMA.**

6.How interrupt request from multiple devices can be handled(APRIL/MAY'2011)

An I/O Device Request An Interrupt By Activating A Bus Line Called Interrupt Request

- SINGLE LEVEL
- MULTI LEVEL

7. What are the components of I/O interface? (Nov/Dec'2011)

We have 3 Bus standards.They are,

- **PCI (**Peripheral Component Inter Connect)
- **SCSI** (Small Computer System Interface)
- **USB** (Universal Serial Bus)

PCI defines an expansion bus on the motherboard.

SCSI and **USB** are used for connecting additional devices both inside and outside the computer box.

SCSI bus is a high speed parallel bus intended for devices such as disk and video display.

USB uses a serial transmission to suit the needs of equipment ranging from keyboard to game control to internal connection.

8.Mention the advantage of USB bus(MAY/JUNE2009)

USB helps to add many devices to a computer system at any time without opening the computer box.

9.What are the i/o data transfer method using memory busses(MAY/JUNE2009)

Three methods used for data transfer between io devices and cpu

1. program i/o or polling
2. interrupt driven i/o
3. direct memory access

10.What is SCSI?(Nov/Dec'2011)

SCSI refers to the standard bus which is defined by ANSI (American National Standard Institute).

SCSI bus the several options. It may be,

Narrow bus → It has 8 data lines & transfers 1 byte at a time.
Wide bus →It has 16 data lines & transfer 2 byte at a time.
Single-Ended Transmission →Each signal uses separate wire.
HVD (High Voltage Differential) → It was 5v (TTL cells)
LVD (Low Voltage Differential) →it uses 3.3v

16 MARKS

1. Design parallel priority interrupt hardware for a system with eight interrupt source. (MAY/JUNE 2007)

INTERRUPTS

When a program enters a wait loop, it will repeatedly check the device status. During this period, the processor will not perform any function.

The Interrupt request line will send a hardware signal called the interrupt signal to the processor.

On receiving this signal, the processor will perform the useful function during the waiting period.

The routine executed in response to an interrupt request is called **Interrupt**

Single interrupt-Diagram
Multiple interrupt-diagram

Vectored Interrupt:

Here the device requesting an interrupt may identify itself to the processor by sending a special code over the bus & then the processor start executing the ISR.

The code supplied by the processor indicates the starting address of the ISR for the device.

The code length ranges from 4 to 8 bits.

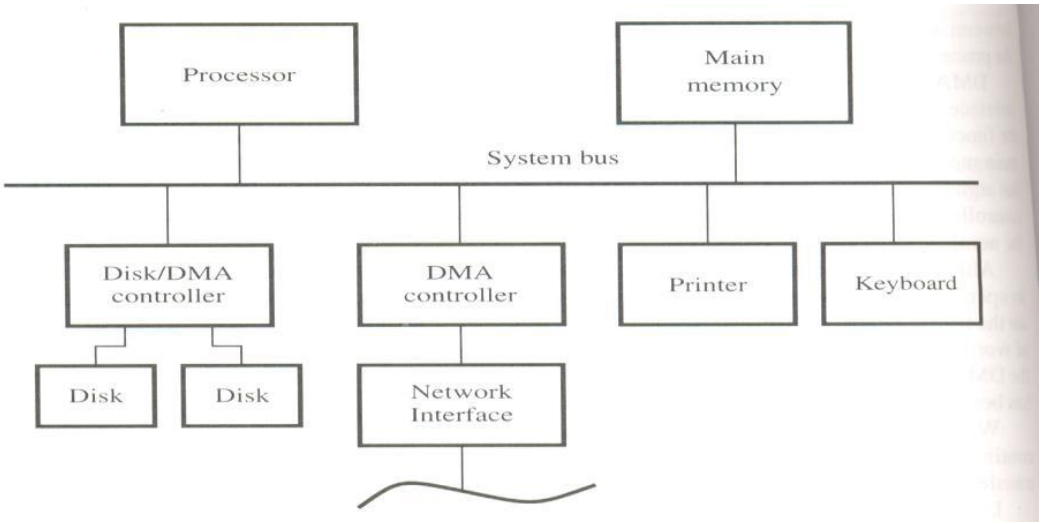
The location pointed to by the interrupting device is used to store the staring address to ISR.

Interrupt Nesting:
Multiple Priority Scheme:

In multiple level priority scheme, we assign a priority level to the processor that can be changed under program control.
The priority level of the processor is the priority of the program that is currently being executed.
The processor accepts interrupts only from devices that have priorities higher than its own.
At the time the execution of an ISR for some device is started,

2. Explain how DMA transfer is accomplished with a neat diagram.(NOV/DEC 2006)

A special control unit may be provided to allow the transfer of large block of data at high speed directly between the external device and main memory , without continous intervention by the processor. This approach is called **DMA.**



Cycle Stealing:

Requests by DMA devices for using the bus are having higher priority than processor requests . Top priority is given to high speed peripherals such as ,

- Disk
- High speed Network Interface and Graphics display device.
- Since the processor originates most memory access cycles, the DMA controller can be said to steal the memory cycles from the processor.

This interviewing technique is called **Cycle stealing.**

Bus Arbitration:

It is the process by which the next device to become the bus master is selected and the bus mastership is transferred to it.

Types:

There are 2 approaches to bus arbitration. They are,
Centralized arbitration (A single bus arbiter performs arbitration)
Distributed arbitration

3. Explain the following

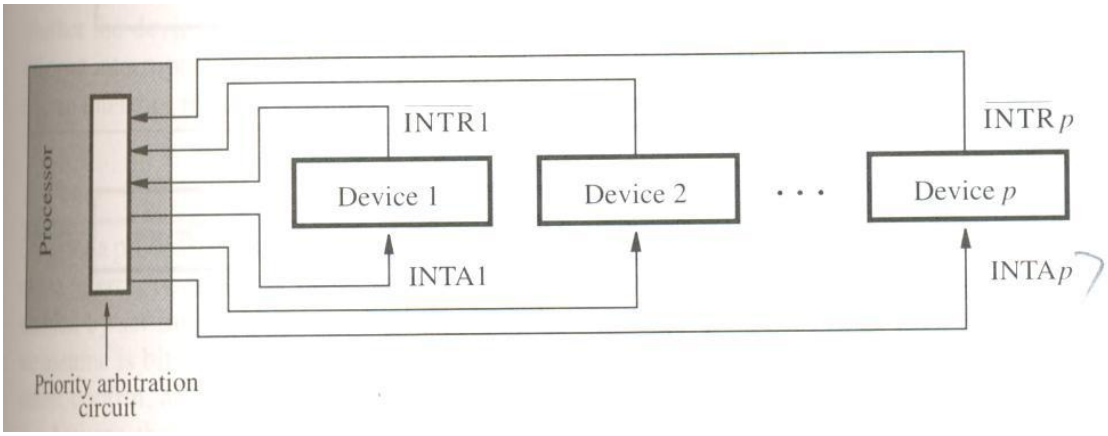
- Memory mapped i/o
- I/O Register
- Hardware Vector Interrupts
- Interrupts

4. Explain the use of vectored interrupts in processors. Why is priority handling desired in interrupt controllers? How do the different priority schemes work? (MAY/JUNE 2006)

- Interrupt hardware
- Single level interrupt-diagram
- Multilevel interrupt- diagram
- Vector interrupt-diagram

Interrupt nesting

Interrupt priority



5. Bus Arbitration Explain different mechanisms used for bus arbitration. (NOV/DEC 2007)

Bus Arbitration:

It is the process by which the next device to become the bus master is selected and the bus mastership is transferred to it.

Types:

There are 2 approaches to bus arbitration. They are,

- Centralized arbitration (A single bus arbiter performs arbitration)
- Distributed arbitration (all devices participate in the selection of next bus master).

Centralized Arbitration:

Here the processor is the bus master and it may grants bus mastership to one of its DMA controller.

A DMA controller indicates that it needs to become the bus master by activating the Bus Request line (BR) which is an open drain line.

The signal on BR is the logical OR of the bus request from all devices connected to it.

When BR is activated the processor activates the Bus Grant Signal (BGI) and indicated the DMA controller that they may use the bus when it becomes free.

This signal is connected to all devices using a daisy chain arrangement.

If DMA requests the bus, it blocks the propagation of Grant Signal to other devices and it indicates to all devices that it is using the bus by activating open collector line, Bus Busy (BBSY).

Fig:A simple arrangement for bus arbitration using a daisy chain

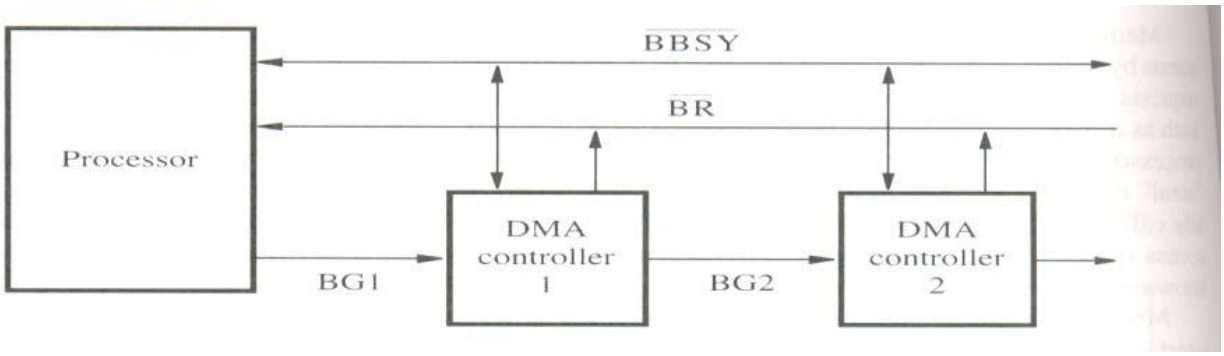


Fig: Sequence of signals during transfer of bus mastership for the devices

The timing diagram shows the sequence of events for the devices connected to the processor is shown.

DMA controller 2 requests and acquires bus mastership and later releases the bus.

During its tenure as bus master, it may perform one or more data transfer.

After it releases the bus, the processor resources bus mastership

Distributed Arbitration:

It means that all devices waiting to use the bus have equal responsibility in carrying out the arbitration process.

Fig: A distributed arbitration scheme