

A.R ENGINEERING COLLEGE, VILLUPURAM DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

SUB.CODE : CS2253 SUB.NAME : COMPUTER ORGANIZATION AND ARCHITECTURE

UNIT-I

BASIC STRUCTURE OF COMPUTERS

PART-A

1.Define Computer Architecture

2. Define Computer H/W

3. What are the functions of control unit ?

4. What is an interrupt?

5. What are the uses of interrupts?

6. What is the need for reduced instruction chip?

7. Name any three of the standard I/O interface.

8. Differentiate between RISC and CISC

9. Explain the various classifications of parallel structures.

10. What is absolute addressing mode?

11. Specify three types of data transfer techniques.

12. What is the role of MAR and MDR?

13. What are the various types of operations required for instructions?

14. What is the role of IR and PC?

15. What are the various units in the computer?

16. What is an I/O channel?

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YEAR/SEM: II/IV

17. What is a bus?

18. Define word length?

19. Explain the following the address instruction?

20. Zero address instruction.

21. What is the straight-line sequencing?

22. What is the role of PC?

23. Define Signal

24. Define Gates

25. Flip flop

26. State and explain the performance equation?

27. Define CPI

29. Define MIPS Rate:

30. Define Throughput and Throughput rate.

PART-B

1. Explain the block diagram of a simple computer with five functional units	(16)
2. a. What is RISC? Explain with proper example.	(8)
b. What is CISC? Explain with proper example.	(8)
3. What are the techniques used to measure the performance of a computer?	(8)
4. What do you mean by addressing modes? Explain various addressing modes	
with the help of examples.	(16)
5. Discuss about Instruction and Instruction sequencing in detail.	(16)
6. Explain in detail about Floating point operations.	(16)

<u>UNIT-II</u>

BASIC PROCESSING UNIT

PART-A

- 1. Specify the sequence of operation involved when an instruction is executed.
- 2. Define parallel processing.
- 3. Define sequential circuits.
- 4. Define interface.
- 5. Define processor clock.
- 6. Define latency.
- 7. Define bandwidth.
- 8. Define hit rate.
- 9. Define miss rate.
- 10. Define Clock Rate:
- 11. Define Throughput:
- 12. Different types of buses.
- 13. What is micro programming and micro programmed control unit?
- 14. What is meant by hardwired control?
- 15. What is Register Renaming?
- 16. What is the function of commitment unit?
- 17. What is the necessity of grouping signals?
- 18. List the techniques used for grouping of the control signals?
- 19 List out Various branching technique used in micro program control unit?
- 20. Define the term Clock Rate.
- 21. What do you mean by out-of order execution? Is it Desirable?
- 22. Define Overflow
- 23. Define Underflow
- 24. What are Condition Codes (CC)? Explain the use of them.
- 25. What is straight -line sequencing?

PART-B

1. a) How will you perform arithmetic or logic operation?	(8)
b) How to fetch a word from memory and store a word in memory?	(8)
2. What is meant by hardwired control? Draw and explain typical hardwire	
control unit.	(16)
3. What is meant by microprogramming?Draw and explain the microprogrammed	
control unit.	(16)
4. List the advantages and disadvantages of micro programmed control unit over	
hardwire control unit.	(16)
5. Discuss in detail about the Multiple bus organization.	(16)

<u>UNIT-III</u>

PIPELINING

PART-A

1. Define pipelining.

2. Define parallel processing.

3. Define instruction pipeline.

4. What are the steps required for a pipelinened processor to process the instruction?

5. What are Hazards?

6. State different types of hazards that can occur in pipeline.

7. Define Data hazards

8. Define Instruction hazards

9. Define Structural hazards?

10. What are the classification of data hazards?

11. Define RAW hazard : (read after write)

12. Define WAW hazard :(write after write)

13. Define WAR hazard :(write after read)

14. How data hazard can be prevented in pipelining?

- 15. How Compiler is used in Pipelining?
- 16. How addressing modes affect the instruction pipelining?
- 17. What is locality of reference?
- 18. What is the need for reduced instruction chip?
- 19. Define memory access time?
- 20. Define memory cycle time.
- 21. Define Static Memories.
- 22. List out Various branching technique used in micro program control unit?
- 23. How the interrupt is handled during exception?
- 24. List out the methods used to improve system performance.
- 25. What is DMA?

PART-B

1. State and explain the different types of hazards that can occur in a pipeline.	(16)
2 .Draw and explain the structure of a superscalar processor. Also explain the flow of	
instruction execution in it.	(16)
3. what are the two aspects of machine instruction? Explain it .	(16)
4. Draw and explain the modified three-bus structure of the processor suitable for	
four – stage pipelined execution. How this structure is suitable to provide four-stage	
pipelined execution?	(16)

UNIT-IV

MEMORY SYSTEM PART-A

- 1. Give the classification of the Optical Media
- 2. What is a Mini Disk?
- 3. List some applications for WORM.
- 4. What are multifunctional drives
- 5. What are types of technology used in s multifunctional drive?
- 6. What is Migration and Archiving?
- 7. How do we use a jukebox?
- 8. List a few requirements imposed by advanced multimedia applications
- 9. What is the use of High water marks in a cache?
- 10. What are the various cache usage in a LAN -based system?
- 11. What are the multimedia applications which use caches?
- 12. Explain virtual memory technique.
- 13. What are virtual and logical addresses?
- 14. Define translation buffer.
- 15. What is branch delay slot?
- 16. What is optical memory?
- 17. What are static and dynamic memories?
- 18. What are the components of memory management unit?
- 19. What is the role of MAR and MDR?
- 20. Distinguish Between Static RAM and Dynamic RAM?
- 21. Distinguish between asynchronies DRAM and synchronous RAM.
- 22. What do you mean associative mapping technique?
- 23. What is SCSI?
- 24. What are the two types of latencies associated with storage?
- 25. What are the data management activities involved in a storage?

- 27. What do you mean by Disk Spanning?
- 28. List some objectives for using RAID Systems
- 29. What are the different levels RAID?
- 30. Two Types of storage devices.

PART-B

1. Define cache memory. Explain the mapping process followed in cache memory. Also	
discuss the relative advantages and disadvantages of the mapping techniques used.	(16)
2. What is virtual memory? Why is it necessary to implement virtual memory? Explain	the
virtual memory address translation.	(16)
3. Draw and explain the various types of secondary storage devices.	(16)
4. a) Explain about RAM.	(8)
b) Explain about ROM.	(8)
5. Discuss in detail about various kinds of memory management schemes.	(16)

<u>UNIT-V</u>

I/O ORGANIZATION

PART-A

- 1. Explain very briefly about ESDI Hard Drive
- 2. Explain in brief about IDE
- 3. What is SCSI?
- 4. Define the term RELIABILITY
- 5. Define the term AVAILABLITY:
- 6. How the interrupt is handled during exception?
- 7. What is IO mapped input output?
- 8. Specify the three types of the DMA transfer techniques?

- 9. What is an interrupt?
- 10. What are the uses of interrupts?
- 11. Define vectored interrupts.
- 12. Name any three of the standard I/O interface.
- 13. What is an I/O channel?
- 14. What is a bus?
- 15. Define word length?
- 16. Why program controlled I/O is unsuitable for high-speed data transfer?
- 17. What is the function of i/o interface?
- 18. What is NUBUS?
- 19. Name some of the IO devices.
- 20. What are the steps taken when an interrupt occurs?
- 21. Define interface.
- 22. What is programmed I/O?
- 23. Types of buses.
- 24. Define Synchronous bus.
- 25. Define Asynchronous bus.

PART-B

1. List the different types of interrupts. Explain briefly about mask able interrupt.	(16)
2. What is DMA? Explain the block diagram of DMA .Also describe how DMA is	
Used to transfer data from peripherals.	(16)
3. Explain the features of USB, PCI, and SCSI bus.	(16)
4. Discuss in detail about.	
a. Buses	(8)
b. Interface circuits	(8)
5. Discuss about I/O devices and processors in detail.	(16)