Two Marks

UNIT I

1.What is cache memory?

The small and fast RAM units are called as caches. when the execution of an instruction calls for data located in the main memory, the data are fetched and a copy is placed in the cache. Later if the same data is required it is read directly from the cache.

2. What is the function of ALU?

Most of the computer operations(arithmetic and logic) are performed in ALU.The data required for the operation is brought by the processor and the operation is performed by the ALU.

3. What is the function of CU?

The control unit acts as the nerve center,that coordinates all the computer operations. It issues timing signals that governs the data transfer.

4. What are basic operations of a computer?

The basic operations are READ and WRITE.

5. What are the registers generally contained in the processor?

MAR-Memory Address Register
MDR-Memory Data Register
IR-Instruction Register
R0-Rn-General purpose Registers
PC-Program Counter

6. What are the steps in executing a program?

1.Fetch
2.Decode
3.Execute
4.Store

7. Define interrupt and ISR?

An interrupt is a request from an I/O device for service by the processor. The processor provides the requested service by executing the interrupt service routine.

8. Define Bus?

A group of lines that serves as a connecting path for several devices is called a bus.

9. What is the use of buffer register?

The buffer register is used to avoid speed mismatch between the I/O device and the processor.

10. Compare single bus structure and multiple bus structure?

A system that contains only one bus(i.e only one transfer at a time) is called as a single bus structure. A system is called as multiple bus structure if it contains multiple buses.

11. What is System Software? Give an example?

It is a collection of programs that are executed as needed to perform functions such as

- Receiving and interpreting user commands
- Entering and editing application programs and storing them as files in secondary storage devices.

Ex: Assembler, Linker, Compiler etc

12.What is Application Software? Give an example?

Application programs are usually written in a high-level programming language, in which the programmer specifies mathematical or text-processing operations. These operations are described in a format that is independent of the particular computer used to execute the program.

Ex: C, C++, JAVA

13. What is a compiler?

A system software program called a compiler translates the high-level language program into a suitable machine language program containing instructions such as the Add and Load instructions.

14. What is text editor?

It is used for entering and editing application programs. The user of this program interactively executes command that allow statements of a source program entered at a keyboard to be accumulated in a file.

15. Discuss about OS as system software?

OS is a large program,or actually a collection of routines, that is used to control the sharing of and interaction among various computer units as they execute application programs.The OS routines perform the tasks required to assign computer resources to individual application programs.

16. What is multiprogrraming or multitasking?

The operating system manages the concurrent execution of several application programs to make the best possible uses of computer resources.this pattern of concurrent execution is called multiprogrraming or multitasking.

17.What is elapsed time of computer system?

The total time to execute the total program is called elapsed time.it is affected by

the speed of the processor,the disk and the printer.

18. What is processor time of a program?

The periods during which the processor is active is called processor time of a Program It depends on the hardware involved in the execution of individual machine instructions.

19. Define clock rate?

The clock rate is given by,
R=1/P,where P is the length of one clock cycle.

20. Write down the basic performance equation?

T=N*S/R
T=processor time
N=no of instructions
S=no of steps
R=clock rate

21.What is pipelining?

The overlapping of execution of successive instructions is called pipelining.

22. What is byte addressable memory?

The assignment of successive addresses to successive byte locations in the memory is called byte addressable memory.

23. What is big endian and little endian format?

The name big endian is used when lower byte addresses are used for the more significiant of the word.The name little endian is used for the less significiant bytes of the word.

24. What is a branch instruction?

Branch instruction is a type of instruction which loads a new value into the program counter.

25. What is branch target?

As a result of branch instructions , the processor fetches and executes the instruction at a new address called branch target, instead of the instruction at the location that follows the branch instruction in sequential address order.

26.What are condition code flags?

The processor keep track of information about the results of various operations for use by subsequent conditional branch instructions. This is accomplished by recording the required information in individual bits, often called condition code flags.

27.Define addressing mode.

The different ways in which the location of an operand is specified in an instruction are referred to as addressing modes.

28.Define various addressing modes.

The various addressing modes are

1.Absolute addressing mode
2.Register addressing mode
3.Indirect addressing mode
4.Index addressing mode
5.Immediate addressing mode
6.Relative addressing mode
7.Autoincrement addressing mode
8.Autodecrement addressing mode

29.What is a pointer?

The register or memory location that contains the address of an operand is called a pointer.

30.What is index register?

In index mode the effective address of the operand is generated by adding a constant value to the contents of a register. The register used may be either a special register or may be any one of a set of general purpose registers in the processor. This register is referred to as an index register.

31.What is assembly language?

A complete set of symbolic names and rules for the use of machines constitute a programming language, generally referred to as an assembly language.

32.What is assembler directive?

SUM EQU 200

Assembler directives are not instructions that will be executed .It simply informs the assembler that the name SUM should be replaced by the value 200 wherever it appears in the program, such statements are called as assembler directives.

33.What is loader ?

Loader is a system software which contains a set of utility programs. It will load the object program to the memory.

34.Define device interface.

The buffer registers DATAIN and DATAOUT and the status flags SIN and SOUT are part of circuitry commonly known as a device

interface.

UNIT II

1.Give the symbol of a full adder circuit for a single stage addition

2.Give the representation for n bit ripple carry adder

3.What is the delay encountered for Cn-1, Sn-1 and Cn in the FA for a single stage

Cn-1 – 2(n-1)
Sn-1 – 2(n-1)+1
Cn – 2n

4.What is the delay encountered for all the sum bits in n-bit binary addition/subtraction logic unit?

The gate delays with and without overflow logic are 2n+2 and 2n respectively

5.Write down the basic generate and propagate functions for stage i

Gi = XiYi, Pi=Xi xor with Yi

6.Write down the general expression for Ci+1 using first level generate and propagate function

Ci+1 = Gi+PiGi-1+PiPi-1Gi-2+…+PiPi-1…P1G0+PiPi-1…P0G0

7.What are the two approaches to reduce delay in adders

- Fastest electronic technology in implementing the ripple carry logic design
- Augmented logic gate network

8.What is the delay encountered in the path in an n x n array multiplier

The delay encountered in the path in an n x n array multiplier is 6(n-1)-1

9.What is skipping over of one's in Booth decoding?

The Transformation 011… 110= +100…0 – 10 is called skipping over one's.In this case multiplier has its ones grouped into a few contiguous blocks.

10.What are the two attractive features of Booth algorithm

- It handles both positive and negative multipliers uniformly
- It achieves some efficiency in the number of additions required when the multiplier has a few large blocks of ones

11. Give an example for the worst case of Booth algorithm

The worst case is shown as below

0 1 0 1 0 1 0 1 0

+1 -1 +1 -1 +1 -1 +1 -1 +1

In the worst case each bit of the multiplier selects the summands. This results in more number of summands.

12. What are the two techniques for speeding up the multiplication operation?

- Bit Pair recoding
- CSA

13. How bit pair recoding of multiplier speeds up the multiplication process?

It guarantees that the maximum number of summands that must be added is n/2 for n bit operands.

14. How CSA speeds up multiplication?

It reduces the time needed to add the summands. Instead of letting the carries ripple along the rows, they can be saved and introduced into the next row, at the correct waited position.

15. Write down the levels of CSA steps needed to reduce k summands to two vectors in CSA The number of levels can be shown by $1.7\log_2 k-1.7$

16. Write down the steps for restoring division and non-restoring division

Non Restoring:

Step1: Do the following n times

1.If the sign of A is 0, shift A and Q left one bit position and subtract M from A otherwise shift A and Q left and add M to A.

2.Now if the sign of A is 0, set Q0 to 1; otherwise set Q0 to 0

Step 2: If the sign of A is 1, add M to A

Restoring:

- Shift A and Q left one binary position
- Subtract M from A
- If the sign of A is one , set Q0 to 0, add M back to A otherwise set Q0 to 1

17.What is the advantage of non restoring over restoring division?

Non restoring division avoids the need for restoring the contents of register after an successful subtraction.

19.What is the need for adding binary 8 value to the true exponential in floating point
numbers?

This solves the problem of negative exponent. Due to this the magnitude of the numbers can be compared. The excess-x representation for exponents enables efficient comparison of the relative sizes of the two floating point numbers.

20.Briefly explain the floating point representation with an example?

The floating point representation has 3 fields

1.sign bit

2.significiant bits
3.exponent
For example consider 1.11101100110 x 10^5,
Mantissa=11101100110
Sign=0
Exponent=5

21.What are the 2 IEEE standards for floating point numbers?

1.single
2.double

22.What is overflow,underflow case in single precision(sp)?

Underflow-In SP it means that the normalized representation requires an exponent less than -126.
Overflow- In SP it means that the normalized representation requires an exponent greater than +127.

23.What are the exceptions encounted for FP operation?

The exceptions encounted for FP operation are overflow,underflow,/0,inexact and invalid values.

24.What is guard bits?

Guard bits are extra bits which are produced during the intermediate steps to yield maximum accuracy in the final results.

25.What are the ways to truncate guard bits?

1.Chopping
2.Von Neumann rounding
3.Rounding procedure

UNIT III

1) Explain MDR and MAR.

The data and address lines of the external memory bus connected to the internal processor bus via the memory data register, MDR, and the memory address register, MAR, respectively. Register MDR has two inputs and two outputs. Data may be loaded into MDR either from the memory bus or from the internal processor bus. The data stored in MDR may be placed on either bus. The input of MAR is connected to the internal bus, and its output is connected to the external bus.

2) Name two special purpose registers.

Index register
Stack pointer

3) Define data path.

The registers, the ALU, and the interconnecting bus are collectively referred to as the data path.

4) Describe the two control signals used for register transfer.
For each register, two control signals are used to place the contents of that register on the bus or to load data on the bus into the register. The input and output of register Ri are connected to the bus via switches controlled by the signals Ri_{in} and Ri_{out}, respectively. When Ri_{in} is set to 1, the data on the bus are loaded into Ri. Similarly, when Ri_{out} is set to 1, the contents of register Ri are placed on the bus. While Ri_{out} is equal to 0, the bus can be used for transferring data from other registers.

5) Define processor clock.
Processor clock is defined as the time periods in which all operations and data transfers with in the processor take place.

6) What is known as multiphase clocking.
When edge-triggered flip flops are not used, two or more clock signals may be needed to guarantee proper transfer of data. This is known as multiphase clocking.

7) Define MFC.
To accommodate the variability in response time, the processor waits until it receives an indication that the requested read operation has been completed. The control signal used for this purpose is known as Memory-Function-Completed (MFC).

8) What is WMFC.
WMFC is the control signal that causes the processor's control circuitry to wait for the arrival of the MFC signal.

9) What is mean by branch instruction.
A branch instruction is an instruction which replaces the contents of the PC with the branch target address. This address is usually obtained by adding an offset X, which is given in the branch instruction, to the updated value of the PC. The location following a branch instruction is called a branch delay slot.

10) Define register file.
All general purpose registers are combined into a single block called the register file.

11) What are the two approaches used for generating the control signals in proper sequence?
Hardwired control
Microprogrammed control

12) What are the factors determine the control signals?
1.Contents of the control step counter
2.Contents of the instruction register
3.Contents of the condition code flags
4.External input signals, such as MFC and interrupt requests

13) Explain hardwired control.
The control hardwire can be viewed as a state machine that changes from one state to another in every clock cycle, depending on the contents of the instruction register, the condition codes, and the external inputs. The outputs of the state machine are the control signals. The sequence of operations carried out by this machine is determined by the wiring of the logic elements, hence the name “hardwired”.

14) What are the features of the hardwired control.
A controller that uses this approach can operate at high speed. It has little flexibility and the complexity of the instruction set it can implement is limited.

15) What is microprogrammed control?
Microprogrammed control is a scheme in which control signals are generated by a program similar to machine language programs.

16) What is control word?
A control word is a word whose individual bits represent the various control signals.

17) Define microroutine and microinstruction.
A sequence of control words corresponding to the control sequence of a machine instruction constitutes the microroutine for that instruction, and the individual control words in this microroutine are referred to as microinstructions.

18) What is control store?
The microroutines for all instructions in the instruction set of a computer are stored in a special memory called the control store.

19) What is the drawback of assigning one bit position to each control signal?
Assigning individual bits to each control signal results in long microinstructions because the number of required signals is usually large. Moreover, only a few bits are set to 1in any given microinstruction, which means the available bit space is poorly used.

20) Name some register output control signals.
PC_{out}, MDR_{out}, Z_{out}, $Offset_{out}$, $R0_{out}$, $R1_{out}$, $R2_{out}$, $R3_{out}$, and

$TEMP_{out}$

21) What is vertical organization and horizontal organization?
Highly encoded schemes that use compact codes to specify only a small number of control functions in each microinstruction are referred to as a vertical organization. On the other hand, the minimally encoded scheme in which many resources can be controlled with a single microinstruction is called a horizontal organization.

22) Compare vertical organization and horizontal organization.
Vertical organization Horizontal organization
1. Highly encoded schemes
2. Specify only a small
number of control signals.
3. Operating speed is high.
Minimally encoded schemes
Many resources can be controlled.
Operating speed is low.

23) Explain bit-O-Ring technique.
The micro program shows that branches are not always made to a single branch address. This is a direct consequence of combining simple micro routines by sharing common parts. Consider a point in the microprogram sequencing. At this point, it is necessary to chose between actions required by direct and indirect addressing modes. If the indirect mode is specified in the instruction, then the microinstruction in the location 170 is performed to fetch the operand from the memory. If the direct mode is specified, this fetch must be bypassed by branching immediately to location 171. The most efficient way to bypass microinstruction 170 is to have the preceding branch microinstructions specify the address 170 and then use an OR gate to change the least significant bit of this address to 1if the direct addressing mode is involved. This is known as the bit-Oring technique for modifying branch addresses.

24) What is the drawback of microprogrammed control?
It leads to a slower operating speed because of the time it takes to fetch microinstructions from the control store.

25) Define emulation.
Given a computer with a certain instruction set, it is possible to define additional machine instructions and implement them with extra microroutines. Emulation allows us to replace obsolete equipment with more up to date machines. If the replacement computer fully emulates the original one, then no software changes have to be made to run existing programs. Thus, emulation facilitates transitions to new computer systems with minimal disruption.

26) Define pipelining.
Pipelining is an effective way of organizing concurrent activity in a computer system. The processor executes the program by fetching and executing instructions, one after the other.

27) Name the four steps in pipelining.
Fetch: read the instruction from the memory.
Decode: decode the instruction and fetch the source operand.
Execute: perform the operation specified by the instruction.
Write: store the result in the destination location.

28) What is the use of cache memory?
The use of cache memories solves the memory access problem. In particular, when a cache is included on the same chip as the processor, access time to the cache is usually the same as the time needed to perform other basic operations inside the processor. This makes it possible to divide instruction fetching and processing into steps that are more or less equal in duration. Each of these steps is performed by a different pipeline stages, and the clock period is chosen to correspond to the longest one.

29) What is data hazard?
Any condition that causes the pipeline to stall is called a hazard. A data hazard is any condition in which either the source or the destination operands of an instruction are not available at the time expected in the pipeline. As a result some operation has to be delayed, and the pipeline stalls.

30) What are instruction hazards?
The pipeline may also be stalled because of a delay in the availability of an instruction. For example, this may be a result of a miss in the cache, requiring the instruction to e fetched from the main memory. Such hazards are often called control hazards or instruction hazards.

31) What are called stalls?
An alternative representation of the operation of a pipeline in the case of a cache miss gives the function performed by each pipeline stage in each clock cycle. The periods in which the decode unit, execute unit, and the write unit are idle are called stalls. They are also referred to as bubbles in the pipeline.

32) What is structural hazard?
Structural hazard is the situation when two instructions require the use of a given hardware resource at the same time. The most common case in which this hazard may arise is in access to memory.
33) What is said to be side effect?

When a location other than one explicitly named in an instruction as a destination operand is affected, the instruction is said to have a side effect.

34) What is dispatch unit?
A separate unit which we call the dispatch unit, takes instructions from the front of the queue and sends them to the execution unit. The dispatch unit also performs the decoding function.

35) What is branch folding/
The instruction fetch unit has executed the branch instruction concurrently with the execution of other instructions. This technique is referred to as branch folding.

36) What is delayed branching?
A technique called delayed branching can minimize the penalty incurred as a result of conditional branch instructions. The idea is simple. The instructions in the delay slots are always fetched. Therefore, we would like to arrange for them to be fully executed whether or not the branch is taken. The objective is to be able to place useful instructions in these slots. If no useful instructions can be placed in the delay slots, these slots must be filled with NOP instructions.

37) Define speculative execution.
Speculative execution means that instructions are executed before the processor is certain that they are in the correct execution sequence. Hence, care must be taken that no processor registers or memory locations are updated until it is confirmed that these instructions should indeed be executed. If the branch decision indicates otherwise, the instructions and all their associated data in the execution units must be purged , and the correct instructions fetched and executed.

38) What is called static and dynamic branch prediction?
The branch prediction decision is always the same every time a given instruction is executed. Any approach that has this characteristic is called static branch prediction. Another approach in which the prediction decision may change depending on execution history is called dynamic branch prediction.

39) What are condition codes?
In many processors, the condition code flags are stored in the processor status register. They are either set or cleared by many instructions, so that they can be tested by subsequent conditional branch instructions to change the flow of program execution.

40) What are superscalar processors?

Several instructions start execution in the same clock cycle, and the processor is said to use multiple issue. Such processors are capable of achieving an instruction execution throughput of more than one instruction per cycle. They are known as superscalar processors.

41) What is imprecise and precise exception?

Situation in which one or more of the succeeding instructions have been executed to completion is called imprecise exception. Situation in which all subsequent instructions that may have been partially executed are discarded. This is called a precise exception.

42) What is commitment unit?

When out-of-order execution is allowed, a special control unit is needed to guarantee in-order commitment. This is called the commitment unit. It uses a queue called the reorder buffer to determine which instruction should be committed next. Instructions are entered in the queue strictly in program order as they are dispatched for execution.

43) What is a deadlock/

A deadlock is a situation that can arise when two units, A and B, use a shared resource. Suppose that unit B cannot complete its task until unit A completes its task. At the same time, unit B has been assigned a resource that unit A needs. If this happens, neither unit can complete its task. Unit A is waiting for the resource it needs, which is being held by unit b. at the same time, unit B is waiting for unit A to finish before it can release that resource.

UNIT-4

1.What is the maximum size of the memory that can be used in a 16-bit computer and 32 bit computer?

The maximum size of the memory that can be used in a 16-bit computer is 2^{16}=64K memory locations.

The maximum size of the memory that can be used in a 32-bit computer is 2^{32}=4 G memory locations.

2. Define memory access time?

The time required to access one word is called the memory access time.

or

It is the time that elapses between the initiation of an operation and the completion of that operation.

3. Define memory cycle time?

It is the minimum time delay required between the initiation of two successive

memory operations.

Eg. The time between two successive read operations.

4. When is a memory unit called as RAM?

A memory unit is called as RAM if any location can be accessed for a read or write operation in some fixed amount of time that is independent of the location's address.

5. What is MMU?

MMU is the Memory Management Unit. It is a special memory control circuit used for implementing the mapping of the virtual address space onto the physical memory.

6. Define memory cell?

A memory cell is capable of storing one bit of information. It is usually organized in the form of an array.

7. What is a word line?

In a memory cell, all the cells of a row are connected to a common line called as word line.

8. Define static memories?

Memories that consists of circuits capable of retaining their state as long as power is applied is called Static memories.

9.What are the Characteristics of semiconductor RAM memories?

- They are available in a wide range of speeds.
- Their cycle time range from 100ns to less than 10ns.
- They replaced the expensive magnetic core memories.
- They are used for implementing memories.

10.Why SRAMs are said to be volatile?

Because their contents are lost when power is interrupted. So SRAMs are said to be volatile.

11.What are the Characteristics of SRAMs?

SRAMs are fast.
They are volatile.
They are of high cost.
Less density.

12.What are the Characteristics of DRAMs?

Low cost.
High density.
Refresh circuitry is needed.

13.Define Refresh Circuit?
It is a circuit which ensures that the contents of a DRAM are maintained when each row of cells are accessed periodically.

14.Define Memory Latency?
It is used to refer to the amount of time it takes to transfer a word of data to or from the memory.

15.what are asynchronous DRAMs?
In asynchronous DRAMs, the timing of the memory device is controlled asynchronously. A specialised memory controller circuit provides the necessary control signals RAS and CAS that govern the timing.The processor must take into account the delay in the response of the memory. such memories are asynchronous DRAMs .

16.what are synchronous DRAMs?
Synchronous DRAMs are those whose operation is directly synchronized with a clock signal.

17.Define Bandwidth?
When transferring blocks of data, it is of interest to know how much time is needed to transfer an entire block. since blocks can be variable in size it is useful to define a performance measure in terms of number of bits or bytes that can be transferred in one second. This measure is often referred to as the memory bandwidth.

18. What is double data rate SDRAMs?
Double data rates SDRAMs are those which can transfer data on both edges of the clock and their bandwidth is essentially doubled for long burst transfers.

19.What is mother board?
Mother Board is a main system printed circuit board which contains the processor.It will occupy an unacceptably large amount of space on the board.

20.What are SIMMs and DIMMs?
SIMMs are Single In-line Memory Modules. DIMMs are Dual In-line Memory Modules. Such modules are an assembly of several memory chips on a separate small board that plugs vertically into a single socket on the motherboard.

21.What is memory Controller?
A memory controller is a circuit which is interposed between the processor and the dynamic memory. It is used for performing multiplexing of address bits.It provides RAS-CAS timing. It also sends R/W and CS signals to the memory. When used with DRAM chips , which do not have self refreshing capability , the memory controller has to provide all the information needed to control the refreshing process.

22.Differentiate static RAM and dynamic RAM?
Slno Static RAM Dynamic RAM

1. They are fast They are slow
2. They are very expensive They are less expensive
3. They retain their state indefinitely. They donot retain their state indefinitely
4. They require several transistors They require lessno transistors.
5. Low density High density

23. What is Ram Bus technology?
The key feature of Ram bus technology is a fast signaling method used to transfer information between chips. Instead of using signals that have voltage levels of either 0 or Vsupply to represent the logic values, the signals consist of much smaller voltage swings around a reference voltage , vref. Small voltage swings make it possible to have short transition times, which allows for a high speed of transmission.

24. What are RDRAMs?
RDRAMs are Rambus DRAMs. Rambus requires specially designed memory chips. These chips use cell arrays based on the standard DRAM technology. Multiple banks of cell arrays are used to access more than one word at atime. Circuitry needed to interface to the Rambus channel is included on the chip. Such chips are known as RDRAMs.

25.What are the special features of Direct RDRAMs?
- It is a two channel Rambus..
- It has 18 data lines intended to transfer two bytes of data at a time.
- There are no separate address lines.

26.What are RIMMs?
RDRAM chips can be assembled in to larger modules called RIMMs. It can hold upto 16 RDRAMs.

27. Define ROM?
It is a non-volatile memory. It involves only reading of stored data.

28.What are the features of PROM?
- They are programmed directly by the user.
- Faster
- Less expensive
- More flexible.

29.Why EPROM chips are mounted in packages that have transparent window?
Since the erasure requires dissipating the charges trapped in the transistors of memory cells. This can be done by exposing the chip to UV light .

30.What are the disadvantages of EPROM?
The chip must be physically removed from the circuit for reprogramming and its entire contents are erased by the ultraviolet light.

31.What are the advantages and disadvantages of using EEPROM?
The advantages are that EEPROMs do not have to be removed for erasure.Also it is possible to erase the cell contents selectively. The only disadvantage is that different voltages are needed for erasing, writing and reading the stored data.

32. Differentiate flash devices and EEPROM devices.

Slno	Flash devices	EEPROM devices
1.	It is possible to read the contents of a single cell, but it is only possible to write an entire block of cells.	It is possible to read and write the contents of a single cell.
2.	Greater density which leads to higher capacity.	Relatively lower density
3.	Lower cost per bit.	Relatively more cost
4.	Consumes less power in their operation and makes it more attractive for use in portable equipments that is battery driven.	Consumes more power.

33.What is cache memory?
It is a small, fast memory that is inserted between the larger, slower main memory and the processor. It reduces the memory access time.
Processor Cache Main memory

34.Define flash memory?
It is an approach similar to EEPROM technology. A flash cell is based on a single transistor controlled by trapped charge just like an EEPROM cell.

35. What is locality of reference?
Analysis of programs shows that many instructions in localized areas of the program are executed repeatedly during some time period., and the remainder of the program is accessed relatively infrequently. This is referred to as locality of reference. This property leads to the effectiveness of cache mechanism.

36. What are the two aspects of locality of reference?. Define them.
Two aspects of locality of reference are temporal aspect and spatial aspect.
Temporal aspect is that a recently executed instruction is likely to be executed again very soon.The spatial aspect is that instructions in close proximity to a recently executed instruction are also to be executed soon.

37. Define cache line.

Cache block is used to refer to a set of contiguous address locations of some size. Cache block is also referred to as cache line.

38.What are the two ways in which the system using cache can proceed for a write operation?

- Write through protocol technique.
- Write-back or copy back protocol technique.

39. What is write through protocol?

For a write operation using write through protocol during write hit: the cache location and the main memory location are updated simultaneously.
For a write miss: For a write miss, the information is written directly to the main memory.

40. What is write-back or copy back protocol?

For a write operation using this protocol during write hit: the technique is to update only the cache location and to mark it as updated with an associated flag bit, often called the dirty or modified bit. The main memory location of the word is updated later, when the block containing this marked word is to be removed from the cache to make room for a new block. For a write miss: the block containing the addressed word is first brought into the cache, and then the desired word in the cache is overwritten with the new information.

41.When does a read miss occur?

When the addressed word in a read operation is not in the cache, a read miss occur.

42.What is load-through or early restart?

When a read miss occurs for a system with cache the required word may be sent to the processor as soon as it is read from the main memory instead of loading in to the cache. This approach is called load through or early restart and it reduces the processor's waiting period .

43.What are the mapping technique?

- Direct mapping
- Associative mapping
- Set Associative mapping

44.What is a hit?

A successful access to data in cache memory is called hit.

45.Define hit rate?

The number of hits stated as a fraction of all attempted access .

46.What are the two ways of constructing a larger module to mount flash chips on a small
card?

- Flash cards.
- Flash drivers.

47.Describe the memory hierarchy?

Processor
Registers
Primary Cache
Secondary Cache
Main memory
Magnetic disk secondary

48. Define Miss rate.

It is the number of misses stated as a fraction of attempted accesses.

49.Define miss penalty?

The extra time needed to bring the desired information into the cache.

50.Define access time for magnetic disks?

The sum of seek time and rotational delay is called as access time for disks.
Seek time is the time required to move the read/write head to the proper track.
Rotational delay or latency is the amount of time that elapses after the head is positioned over the correct track until the starting position of the addressed sector passes under the read/write head.

51.What is phase encoding or Manchestor encoding?

It is one encoding technique for combining clocking information with data. It is a scheme in which changes in magnetization occur for each data bit. It s diadvantage is poor bit-storage density.

52.What is the formula for calculating the average access time experienced by the processor?

t_{ave}=hc +(1-h)M
Where
h =Hit rate
M=miss penalty
C=Time to access information in the cache.

53. What is the formula for calculating the average access time experienced by the processor in a system with two levels of caches?

$t_{ave} = h_1c_1(1-h_1)h_2c_2+(1-h_1)(1-h_2)M$

where
h_1=hit rate in L_1 cache
h_2=hit rate in L_2 cache
C_1=Time to access information in the L_1 cache.
C_2=Time to access information in the L_2 cache.

54.What are prefetch instructions?
Prefetch Instructions are those instructions which can be inserted into a program either by the programmer or by the compiler.

55.Define system space?
Management routines are part of the operating system of the computer.It is convenient to assemble the OS routines into a virtual address space.

56.Define user space?
The system space is separated from virtual address space in which the user application programs reside. The letter space is called user space.

57.What are pages?
All programs and data are composed of fixed length units called pages.each consists of blocks of words that occupies contiguous locations in main memory.

58.What is replacement algorithm?
When the cache is full and a memory word that is not in the cache is referenced, the cache control hardware must decide which block should be removed to create space for the new block that contains the reference word .The collection of rules for making this decision constitutes the replacement algorithm.

59.What is dirty or modified bit?
The cache location is updated with an associated flag bit called dirty bit.

60.What is writemiss?
During the write operation if the addressed word is not in cache then said to be writemiss.

61.What is associative research?
The cost of an associative cache is higher than the cost of a direct mapped cache because of the need to search all 128 tag patterns to determine whether a given block is in the cache.A search of this kind is called an associative search.

62.What is virtual memory?
Techniques that automatically move program and datablocks into the physical main memory when they are required for execution are called as virtual memory.

63.What is virtual address?
The binary address that the processor used for either instruction or data called as

virtual address.

64.What is virtual page number?
Each virtual address generated by the processor whether it is for an instruction Fetch is interpreted as a virtual page.

65.What is page frame?
An area in the main memory that can hold one page is called as page frame.

66.What is Winchester technology?
The disk and the read/write heads are placed in a sealed air-filtered enclosure called Winchester technology.

67.What is a disk drive?
The electromechanical mechanism that spins the disk and moves the read/write heads called disk drive.

68.What is disk controller?
The electronic circuitry that controls the operation of the system called as disk controller.

69.What is main memory address?
The address of the first main memory location of the block of words involved in the transfer is called as main memory address.

70.What is wordcount?
The number of words in the block to be transferred.

71.What is Error checking?
It computes the error correcting code (ECC)value for the data read from a given sector and compares it with the corresponding ECC value read from the disk.

72.What is booting?
When the power is turned on the OS has to be loaded into the main memory ,which takes place as part of a process called booting.To initiate booting a tiny part of main memory is implemented as a nonvolatile ROM.

73.What are the two states of processor?
- Supervisor state
- User state.

UNIT V

1. what is memory mapped I/O?
Whan the I/O devices share the same address space,the arrangement iscalled memory mapped I/O.

2. What is program controlled I/O?
In program controlled I/O , the processor repeatedly checks a status flag to achieve the required synchronization between the processor and an input and output device

3.what are the various mechanisms for implemernting I/O operations?
- Program controlled I/O
- Interrupts
- DMA

4.what are vectored interrupts?
To reduce the time involved in the polling process,a device requesting an interrupt may identify itself directly to the processor.Then the ,processor can immediately start executing the corresponding ISR.The schemes based on this approach is called vectored interrupts.

5. when the privilege exception arises?
An attempt to execute a privileged instruction while in the user mode leads to a special type of interrupt called a privilege exception.

6.what are the 2 independent mechanisms for controlling interrupt request?
- At the device end,an interrupt enable bit in a control register determines whether the device is allowed to generate an interrupt request.
- At the processor end,either an interrupt enable bit in the PS or a priority structure determines whether a given interrupt request will be accepted.

7.what is time slicing?
With this technique each program runs for a short period called a time slice,then another program runs for its time slice and so on.

8.What is DMA?
Transfer of a block of data directly between an external device and main memory, with out continuous intervention by the processor is called DMA.

9.What is DMA controller?
DMA transfers are performed by a control circuit that is part of the I?O device interface.This cuircuit is known as DMA controller.

10.What is cycle stealing?
The processor originates most memory access cycles and the DMA controller can be said to stael memory cyckles from the processor.This technique is known as cycle stealing.

11.What is bus arbitration?
It is the process by which the next device becomes the bus master is selected and bus master ship is transferred to it.

12 what are the three types of buses?

- Address bus
- Data bus
- Control bus

13.What are the objectives of USB?
- Simple
- Low cost
- Easy to use
- Supports wide range of data transfer characteristics.
- Plug and play mode of operation

14. what is synchronous bus?
In this, all devices derive timing information from a common clock line.

15. what is asynchronous bus?
In this, all devices do not derive timing information from a common clock line. It uses handshake between the master and the slave.